Thesis for the Degree of Master of Engineering

# 12-bit 1MSps SAR ADC for System-on-Chip

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# 12-bit 1MSps SAR ADC for System-on-Chip

## 시스템-온-칩을 위한 12 비트 1MSps SAR ADC

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# 12-bit 1MSps SAR ADC for System-on-Chip

## Abstract

Over the past ten years, as integrated circuits became increasingly more complex and expensive, the industry began to embrace new design and to reuse methodologies that are collectively referred to as System-on-Chip (SoC) design. To solve these problems, analog-to-digital converter (ADC) is required in SoC.

This thesis focuses on the design of successive approximation register (SAR) ADC for SoC. The proposed of SAR ADC contains Sample-and-Hold stage, capacitor array, SAR control logic stage, comparator stage, DAC stage, and DAC control logic stage. This SAR ADC is designed to have performance of 12-bit resolution. The proposed circuit is designed using Magnachip/SK Hynix 0.18μm CMOS 1Poly-6Metal process, and it is powered by 1.5V supply. To reduce chip area and power consumption, we minimized unit capacitor area and number of the total capacitors, and designed the circuit optimization as compared to conventional circuits. The proposed circuit in this thesis showed high signal-to-noise distortion ratio (SNDR) of 71.18dB, and excellent effective number of bit (ENOB) 11.53-bit as compared to conventional research results. The designed circuit also showed very low power consumption of 1.95mW, and small chip area of 0.54mm$^2$. The proposed ADC is applicable for the signal conversion of the industry system application.

# 1 Introduction

Significant resources have been used with the vast performance. The design tasks have interlinked with scheming between the edifice blocks of circuits and the gathering of sufficient supporting circuit logic to comprehend a system-on-chips (SoCs). Soc is the integrated system which integrates all of the system circuits on a single chip. It is the most advanced form which uses powerful processors and various peripherals for running Windows and Linux. SoC consists of the embedded hardware and software which controls processors, controllers and other peripherals [1-3].

Most ADC applications can be classified into four broad market segments such as data acquisition, precision industrial measurement, voice band and audio and high speed system with sampling rates of greater than 5 MSps (5 Mega Sampling per second). A very large percentage of these applications can be filled by successive-approximation register (SAR) ADCs, sigma-delta (Σ-Δ) ADCs, and pipelined ADCs. A basic understanding for the three most popular ADC architectures and their relationship to the market segments is a useful to supplement the selection guides and search engines. The 10-bit flash ADC is mainly the fastest ADC among all the ADC types. In flash ADC of n-bit in size,

($2^n$ -1) comparators and $2^n$ registers are needed. It is very fast as mentioned but it requires for example, many parts of 1023 comparators for 10-bit ADC, lower resolution, expensive cost and large power consumption. Pipeline ADC with a resolution of less than 16 bits has fast sampling rate of tens KHz ~ hundreds MHz but it also has a disadvantage in power consumption. Further, SAR ADC has a resolution similar to the pipelined ADC, and its sampling rate (speed) is a relatively low. However, the SAR ADC has the advantage of reducing the area of the design because of the blocks of the internal recycle. Therefore, the SAR ADC is suitable to have a low power and low area, for designing a 12-bit ADC with a proper resolution. As it can be seen in previous studies, ADC requires development with a low-power and low-area domain consistent with the particular application [4-12].

In this thesis, we propose a SAR ADC with low power and low area. The capacitor array and switched capacitor used in the general structure of the SAR ADC, may occupy a large area. To solve this problem, the capacitor array and sample-and-hold stage with a bootstrap switch are proposed by structural change to reduce the number of capacitors. It is possible to reduce the power consumption due to the reduced capacitor.

In Chapter 2 of this thesis, we explain the basic concept of a common ADC, and describe the operating principle of SAR ADC. Chapter 3 describes the proposed SAR ADC circuit of each stage, for its interpretation. Chapter 4 analyzes the results and performance analysis through implementation and evaluation of the proposed SAR ADC. Chapter 5 finally concludes the result and performance summary of this thesis.

# 2 ADC operation principles and basic concepts

In this chapter, we describe the concept and operating principle of a typical ADC, and describe the performance and characterization of the ADC.

## 2.1 Structure and operating principle of the ADC

Figure 2.1 shows the typical ADC symbol. In electronics, an ADC is a system that converts an analog input signal into a digital output signal, and it is widely used in various industries such as information communication field, the video signal field, medical devices, and the computer filed.

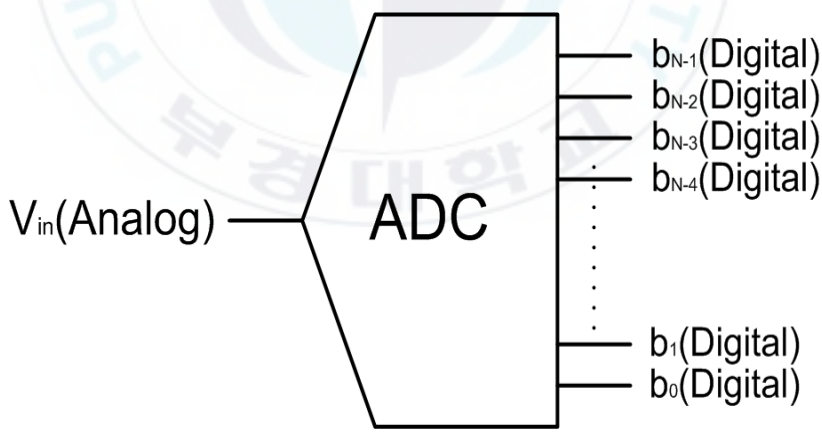



**Figure 2.1 ADC symbol**

Figure 2.2 is conventional ADC system block diagram. When the analog signal is input and the inserted signal is sampled by the sample-and-hold stage for digital encoding, ADC stage receives the sampled signal from sample-and-hold stage, and it provides the digital data to the output latch stage. Output latch part is inserted to solve the problem of the interface and the digital circuit, since the output of the ADC is connected to the data bus, such as a microprocessor. The architectures such as flash ADC, sigma-delta ADC, and SAR ADC are widely used. Each of the ADC may have different suitable structure for the sampling rate and the number of bits.

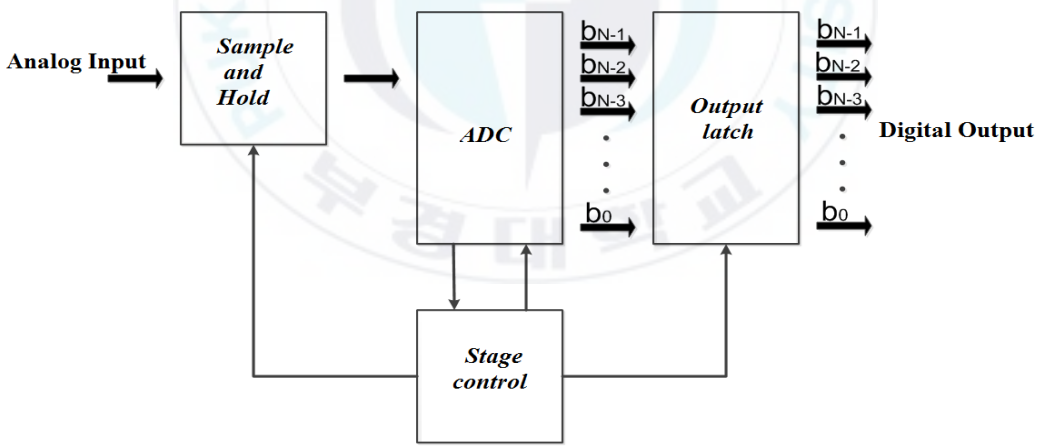



**Figure 2.2 Conventional ADC system block diagram**

Figure 2.3 shows typical ADC with various number of bits and sampling rates.

As shown in Figure 2.3 sigma-delta (Σ-Δ) ADC is 16-bit resolution, for high resolution application, but hundreds of KHz sampling rate of the ADC is not suitable for the SoC. Flash ADC is mainly used in low resolution of less than 10 bits, and the operation speed is fast, but its power consumption is high. Pipeline ADC with a resolution of less than 16 bits, can have a fast sampling rate of tens KHz to hundreds MHz, but its power consumption is also high. The SAR ADC and pipeline ADC have a similar resolution and their sampling rates are relatively low because of recycling the drawbacks of the inner block with low area. Therefore, the SAR ADC is suitable to apply a low power and low-area application for a 12-bit ADC with a proper resolution.

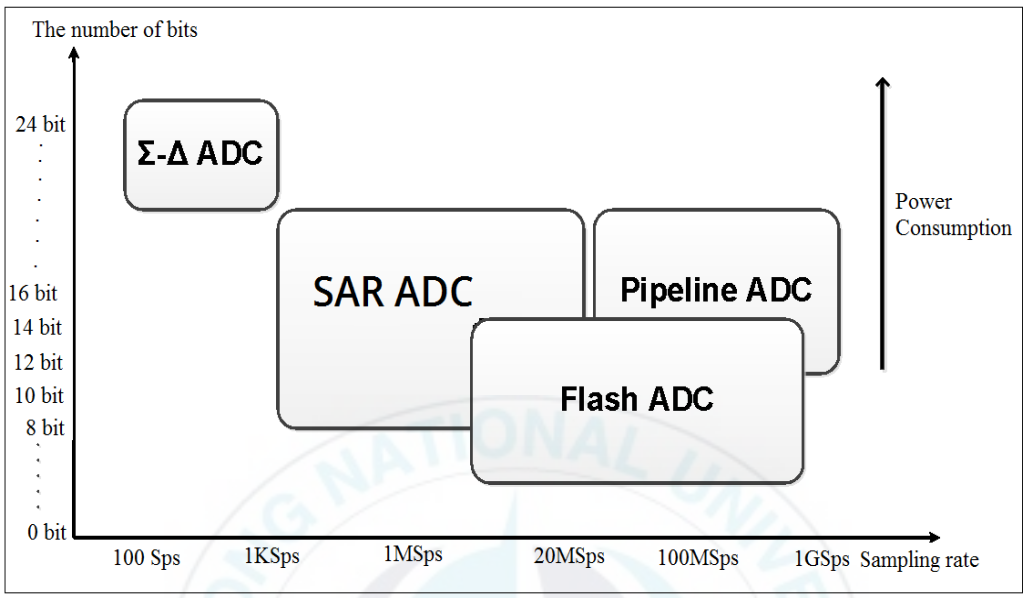



**Figure 2.3 Typical ADC with various bits and sampling rates**

## 2.2 The main performance indices and formulas of the ADC

The important performances of the ADC contain the differential non-linearity (DNL) error, integral non-linearity, (INL) error, signal-to-noise ratio distortion (SNDR), and effective number of bits, (ENOB).

DNL error as shown in Figure 2.4 indicates difference between an ideal step width and the ideal value. For example, if the input voltage width is 1LSB and if the measured voltage width is 1.2LSB, it provides DNL of -0.2 LSB.

INL error in Figure 2.4 is the maximum deviation between the ideal output of a ADC and the actual output level (after offset and gain errors have been removed). Since these errors are closely related to the linearity of the ADC, small errors provide excellent linearity.

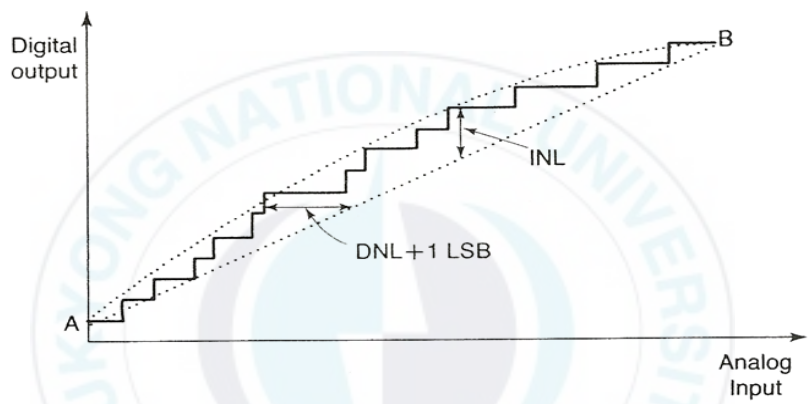



**Figure 2.4 DNL and INL characteristics of ADC**

Equation (2.1) shows signal to noise ratio, SNR.

$$SNR = 6.02N + 1.02 \tag{2.1}$$

where N is the number of bits of resolution of the converter.

SNDR is a measurement of the purity of signal. It is typically used in data

converter specifications. Equation (2.2) expresses ENOB. ENOB is a measure of the dynamic range of an ADC and its associated circuit. ENOB is also used as a quality measure for other blocks such as sample-and-hold stage.

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.2}$$

As can be seen from the equation (2.2), ENOB is used as the most important performance of the ADC.

## 2.3 SAR ADC structure and operation principle

Figure 2.5 shows a block diagram of a general SAR ADC. The SAR ADC consists of sample-and-hold stage, capacitor array network stage, comparator stage, SAR logic stage, control logic stage and the DAC stage. The SAR ADC is a type of ADC that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before

finally converging upon a digital output for each conversion. The sample-and-hold (S/H) is an analog circuit that samples (captures, grabs) the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimum period of time. Successive approximation procedure to perform the charge redistribution operating in the capacitor array network stage is compared with reference voltage at the comparator. The output signal of the comparator is transmitted to the SAR logic using a successive approximation algorithm to determine a digital code of the analog input.

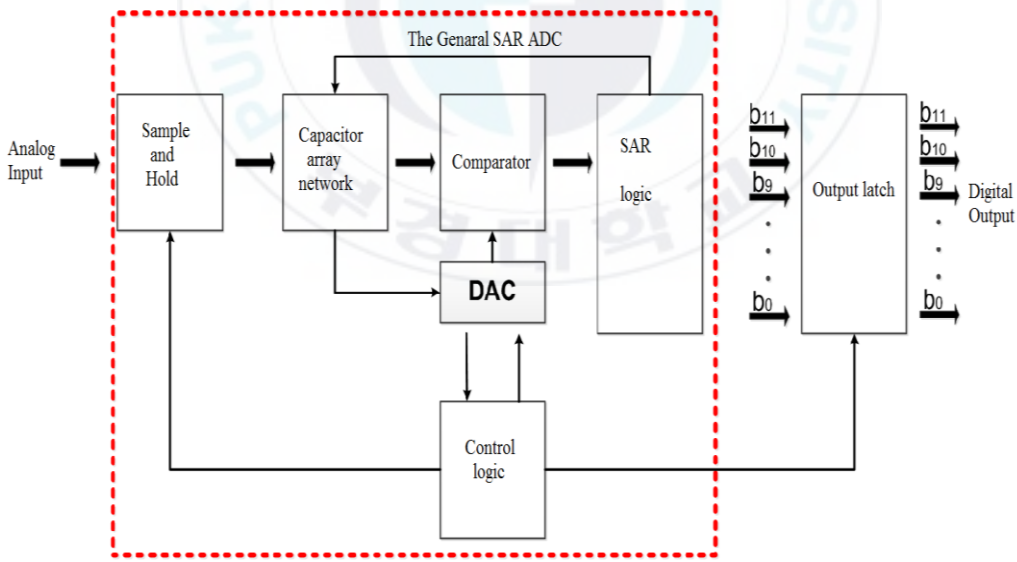



**Figure 2.5 General SAR ADC**

Figure 2.6 shows code decision procedure of 3-bit SAR ADC. The first step converts a digital code to a medium value with the most significant bits (MSB) ‘1’, and less significant bits (LSB) ‘0’ to be transmitted to the DAC. The DAC corresponding to this digital code $V_{DAC}$ using the analog input signal $V_A$ is applied to the comparator. At this time, when the analog input signal $V_A$ is greater than the $V_{DAC}$, MSB sets to ‘0’. If the analog input signal $V_A$ is smaller than the $V_{DAC}$, MSB remains ‘1’. When the algorithm this step it provides binary codes that corresponds to the input voltage. This process is referred to as successive approximation. The produced code results in a readable data form.

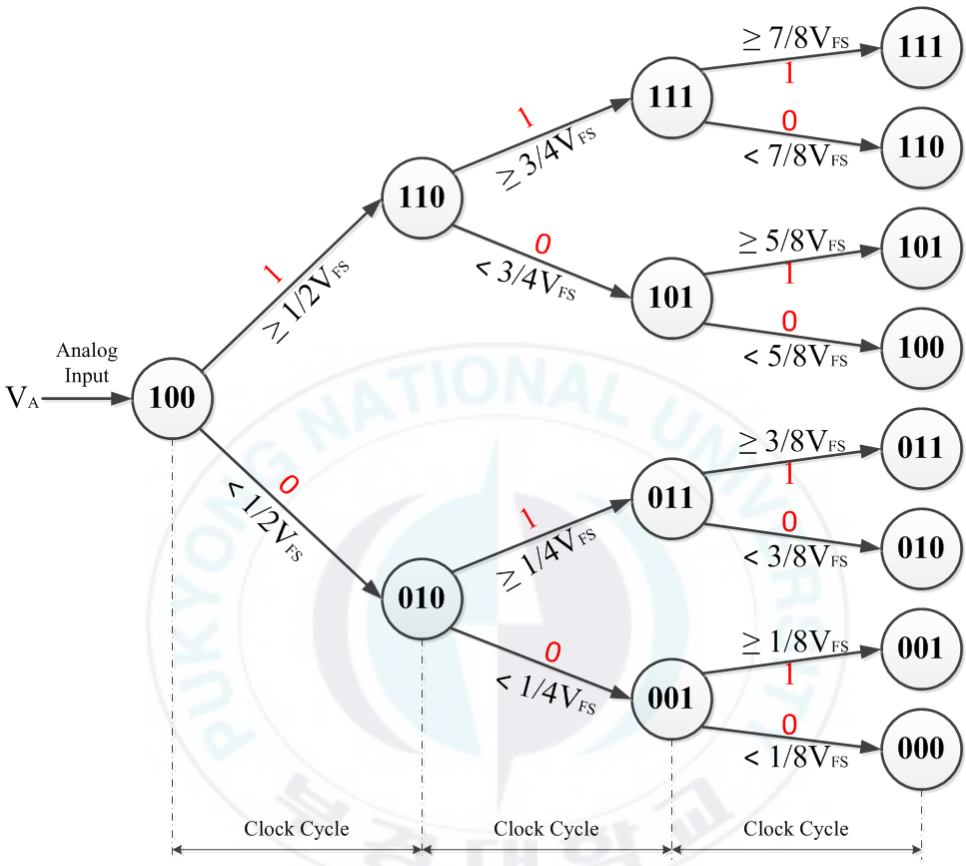



**Figure 2.6 Code decision procedure of 3-bit SAR ADC**

Figure 2.7 shows 3 modes of typical 12-bit charge redistribution SAR ADC. In sample mode of the first step as shown in Figure 2.7(a), since switch $S_A$ is 'on' status, the top plates of the capacitors are short-circuited are connected to ground,

and the bottom plates of the all capacitors are connected to the analog input $V_A$. Therefore, the top plates of all capacitors store which are proportional to $V_A$. Equation (2.3*)* represents $Q_X$ store in all capacitors.

$$Q_X = C_{tot}V_A = 2CV_A \tag{2.3}$$

where $C_{tot}$ is the sum of total capacitors.

In the hold mode, the switch $S_A$ is opened, the switch $S_B$ is connected to the reference voltage $V_{ref}$ and, bottom plates of all capacitors are connected to ground as shown in Figure 2.7(b). At this point since charges charged in the capacitor store their values, top plate voltage $V_X$ provides -$V_A$.

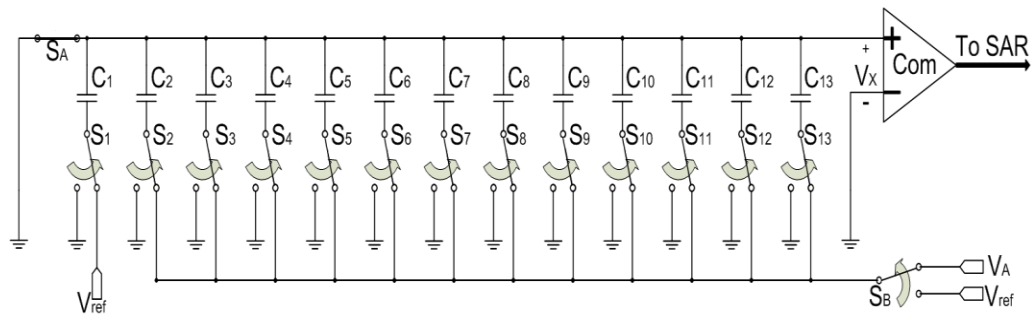
In the redistribution mode, it performs a process of successive approximation as shown in Figure 2.7(c). First switch $S_1$ for the most significant bit (MSB) is connected to the reference voltage $V_{ref}$, and other switches ($S_2$~$S_{13}$) the ground. At this point the capacitor voltage $V_X$ is increased from -$V_A$ to $V_{ref}/2$. This status is expressed by Equations (2.4a), (2.4b) and (2.5). When $Q_i$ is the initial charge in the sample mode, and charge after the switch $S_1$ is connected to the reference voltage $V_{ref}$ $Q_f$, it is expressed by Equations (2.4a) and (2.4b). Let's consider $Q_i$ = $Q_f$. Thus we can get Equation (2.5)

$$Q_i = -2CV_A \tag{2.4a}$$

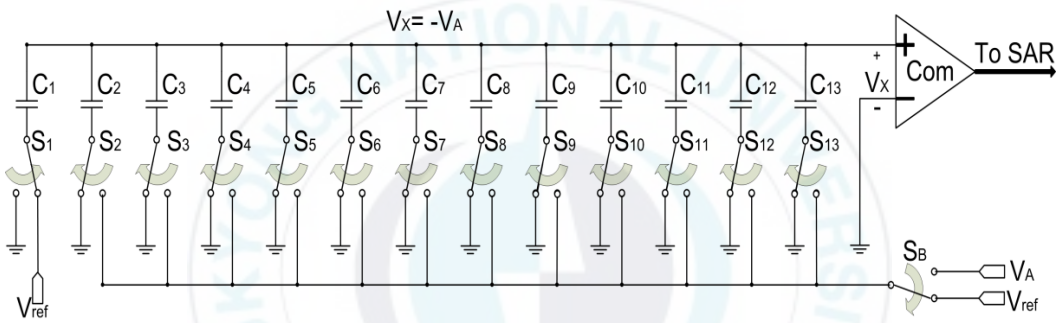
$$Q_f = CV_X + C(V_X - V_{ref}) \tag{2.4b}$$

$$V_X = -V_A + \frac{V_{ref}}{2} \tag{2.5}$$

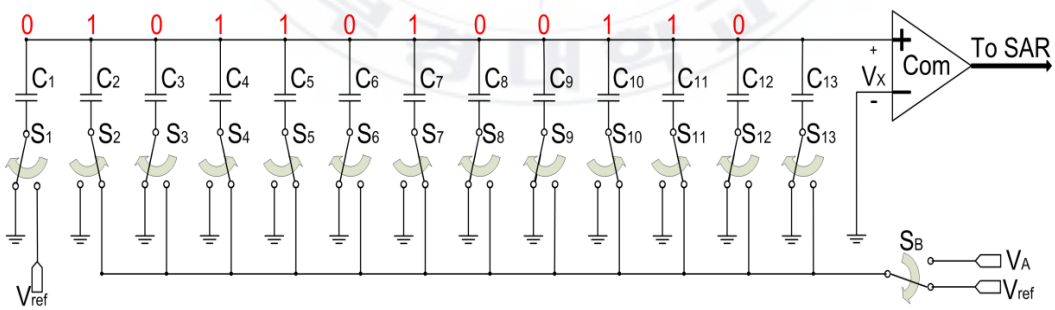
From Equation (2.5), when the value of $V_A$ has a value of greater than $V_{ref}/2$, $V_X$ has a negative value, and so the output of the comparator is a 'Low' status, and thus the switch $S_1$ remains state connected to $V_{ref}$. In this case MSB determines code '1'. On the other hand, when the $V_X$ has a positive value for $V_A$ of less than $V_{ref}/2$, the switch $S_1$ is replaced by a connection from reference voltage $V_{ref}$ to a ground. In such case, the code value of the MSB is determined as '0' status. Therefore this code status procedure is repeatedly performed from switch, $S_2$ to switch $S_{12}$ providing the least significant bit (LSB). In this case the switch $S_{13}$ still remains the ground during the redistribution process.




(a) Sample mode




(b) Hold mode




(c) Redistribution mode

**Figure 2.7 12-bit charge-redistribution SAR ADC**

# 3 The proposed SAR ADC circuit and analysis

This chapter describes each stage of the circuit and the role of SAR ADC.

Figures 3.1 illustrates the block diagram of a SAR ADC including a sample-and-hold, control logic stage, capacitor array network stage, the comparator stage, DAC stage, output latch and SAR logic stage. The proposed SAR ADC includes a sample-and-hold stage and the control logic stage as compared to general SAR ADC.

The circuit design and the role of each stage will be described in the following.

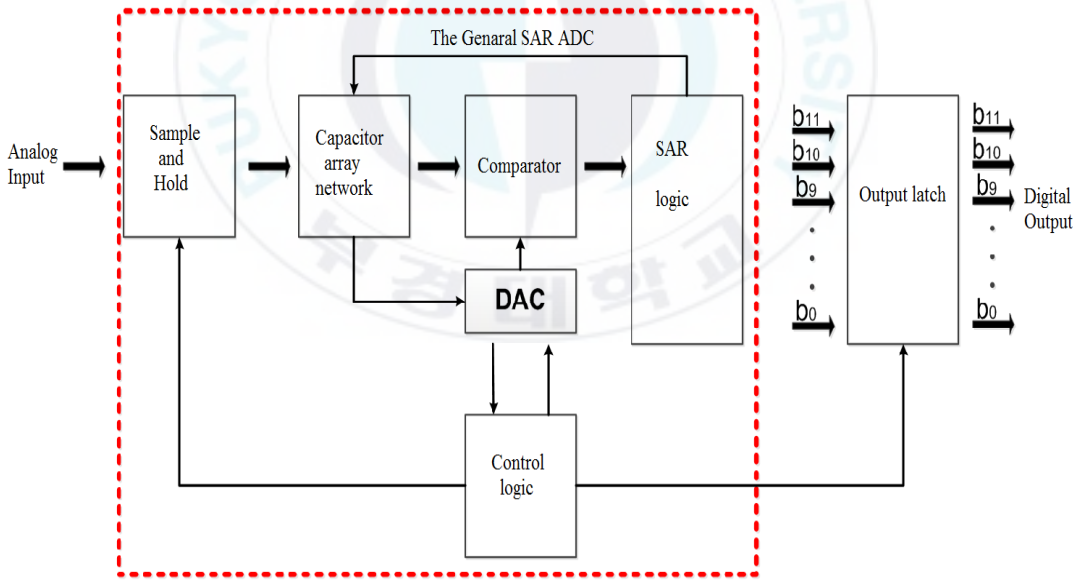



**Figure 3.1 The proposed SAR ADC**

## 3.1 Sample-and-Hold stage

Sample-and-hold stage is an analog device that samples the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimum period of time, and it sends the sampled signal to the capacitor array network stage. Sample-and-hold stage holds the sampled signal at the sampling rate of 1MSps for the sampling of two analog input signals with the phase difference of 180°. Figure 3.2 illustrates schematic of sample-and-hold stage. The input signals contain an analog input signal of '$V_{INT}$' and two control clock signals of *'Clks'* and '*Clksb*'. '$V_+$' signal represents the output signal of the sample-and-hold stage, it has a sampling rate of 1MSps. '$V_+$' signal is transmitted to the capacitor array network stage. As shown in Figure 3.2, the gate-source voltage of $M_7$ is fixed to the supply voltage $V_{DD}$ to improve the linearity of the switch due to the low on-resistance. When the clock control signal *Clks* is 'Low' status and the switch $M_7$ is "off" status, the gates of $M_8$ and $M_9$ are discharge to ground, and so the $V_{DD}$ is applied to the $C_1$ by the $M_{10}$ and $M_2$. $C_1$ is a rechargeable battery role in the "turn-on" state of the switch, $M_3$ and $M_6$ disconnect between $C_1$ and $M_7$ during the charging. When the clock control signal *Clks*, is 'High' switch $M_7$ is 'on' status applied to only the voltage $V_{DD}$ at the gate

and the source. Therefore gate voltage $V_{+G}$ of $M_6$ provides Equation (3.1).

$$V_{G+} = V_{INT} + \frac{C_1}{C_1 + C_p} V_{DD} \tag{3.1}$$

where $C_p$ is the total parasitic capacitance.

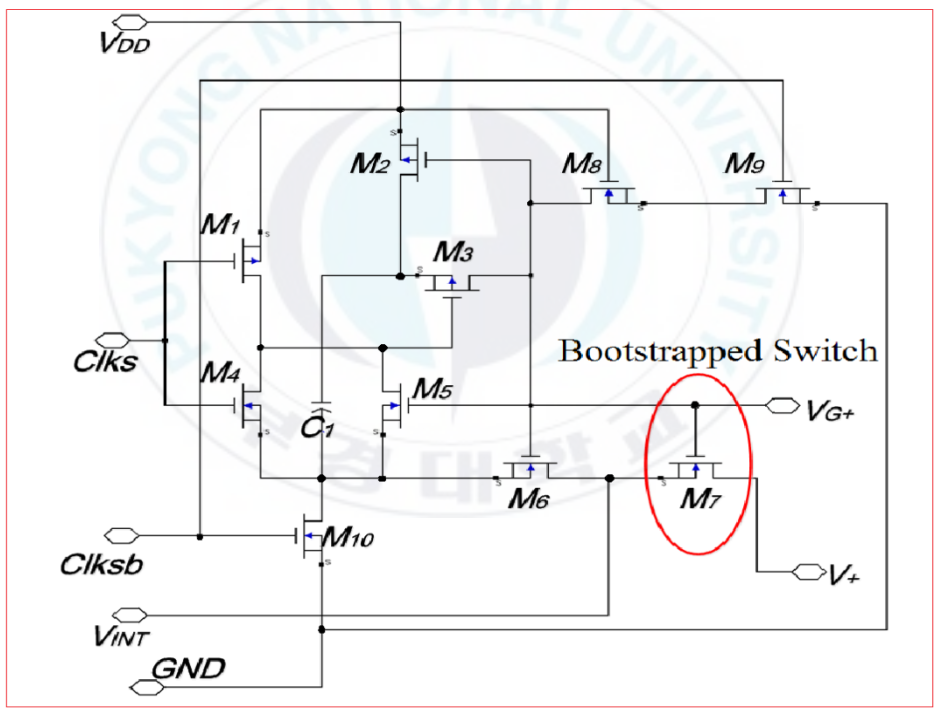



**Figure 3.2 Schematic of sample-and-hold stage**

Figure 3.3 shows the layout of the sample-and-hold stage. Using Cadence Virtuoso program we followed the layout rules of Magnachip/SK Hynix's 1-Poly 6-Metal 0.18μm CMOS process. The proposed sample-and-hold stage showed small area of 85μm × 45μm.

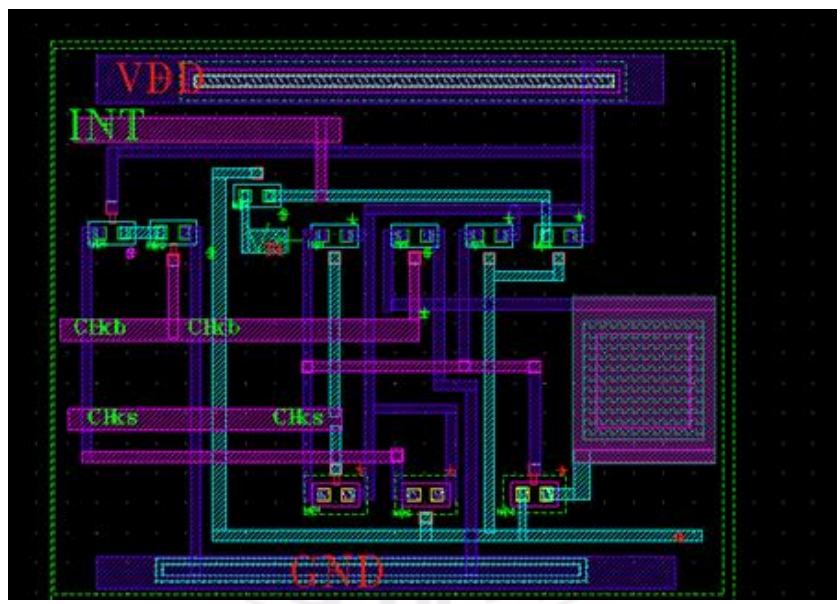



**Figure 3.3 Sample-and-hold stage layout**

## 3.2 Capacitor array network stage

The capacitor array network stage plays role in performing charge redistribution for the sampling and hold to a digital signal of 12 bits signal from the sample-and-hold stage.

Figure 3.4 shows the capacitor array network stage, this stage performs charge redistribution that connects one input of differential inputs applied from the sample-and-hold stage in parallel with the capacitor array of 12 sets. It is composed of two capacitor arrays due to the differential structure, and so it has capacitors of 24 sets. This capacitor array network transfers redistributed signal to comparator stage which will be mentioned in Section 2.

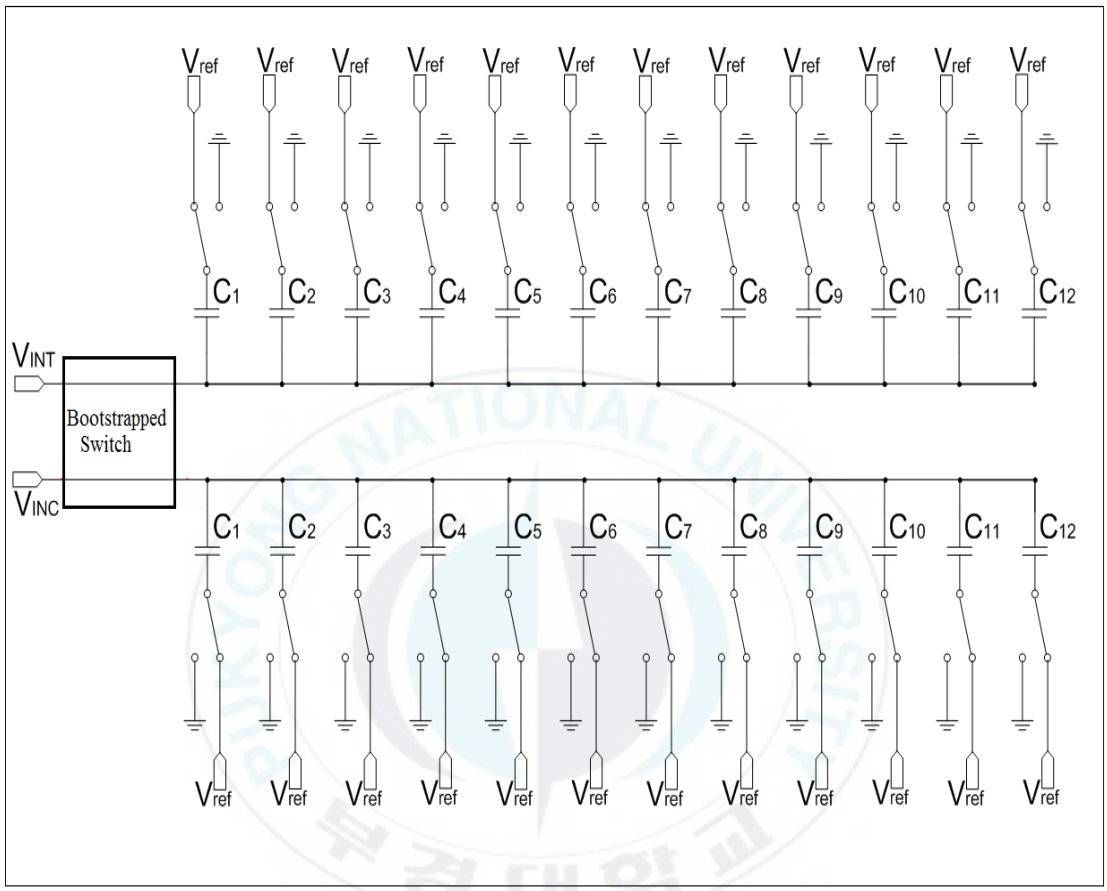
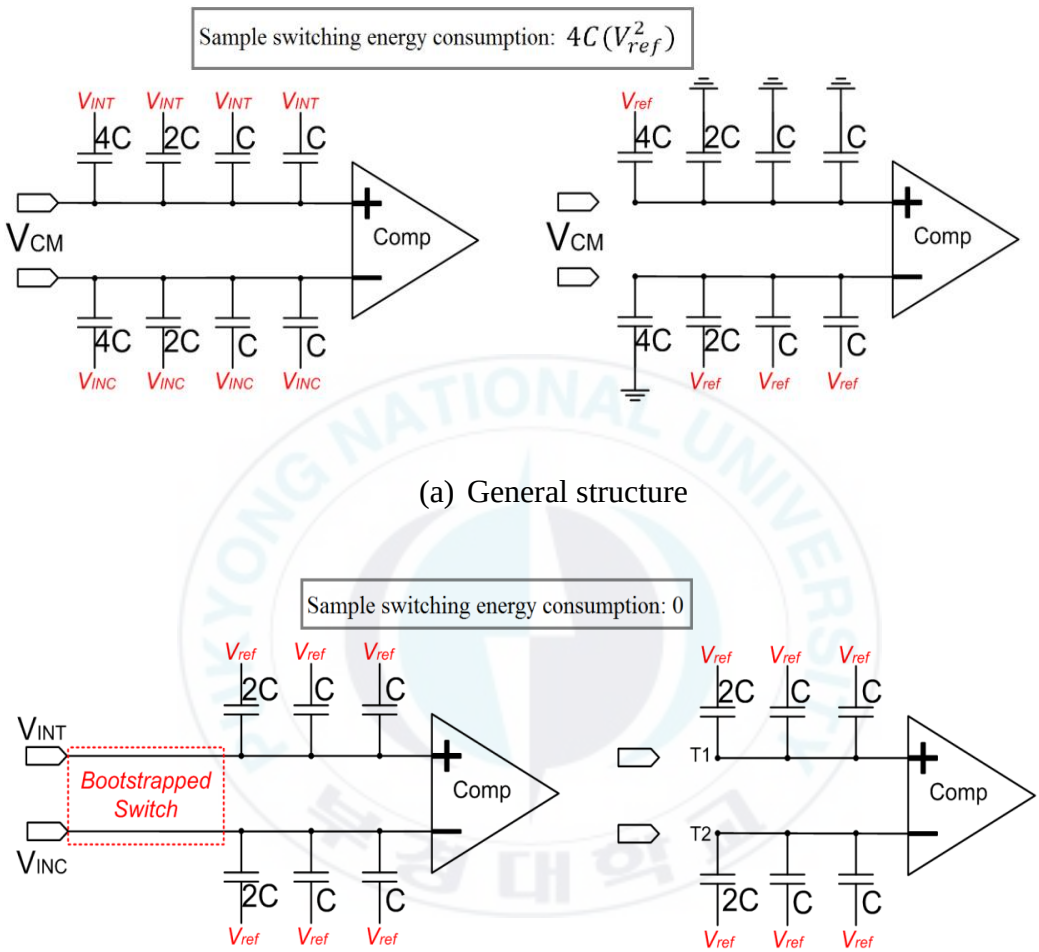



**Figure 3.4 Capacitor array network of proposed SAR ADC**

Figure 3.5 shows a comparison of the structure proposed in this research and the typical structure for a SAR ADC capacitor array network stage. General the SAR ADC capacitor array network of N-bit configures to two arrays with each array per (N + 1) of capacitors configured to connect each network stage in

parallel. In other words, to provide capacitor array with 12-bit resolution, it contains 26 capacitors. The general case as shown in Figure 3.5(a) connects a common-mode voltage '$V_{CM}$' on the top plate of the capacitor in charge redistribution and signal applied from the sample-and-hold stage is connected to the bottom plate of the capacitor array. On the other hand, the proposed capacitor array network as shown in Figure 3.5(b) writhes with bootstrap switches of sample-and-hold stage in Figure 3.2.




(a) General structure

(b) Proposed structure

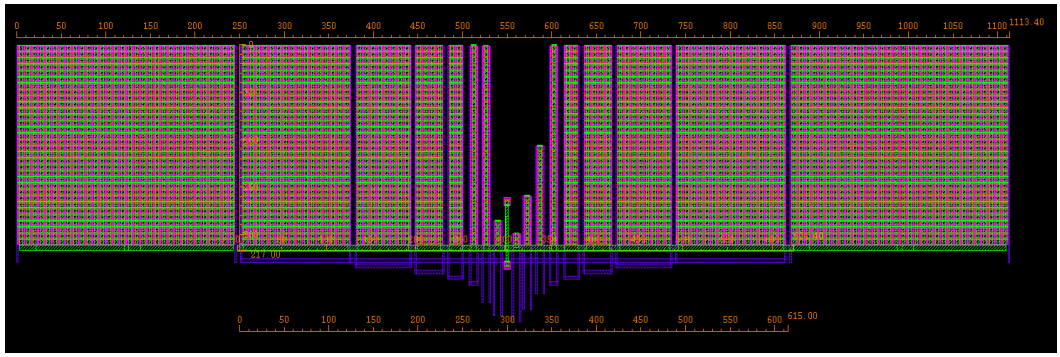
**Figure 3.5 Comparison of SAR ADC capacitor array network stage**

Equation (3.2) describes average switching energy consumption of a general capacitor array network, and Equation (3.3) shows average switching energy consumption of the proposed structure.

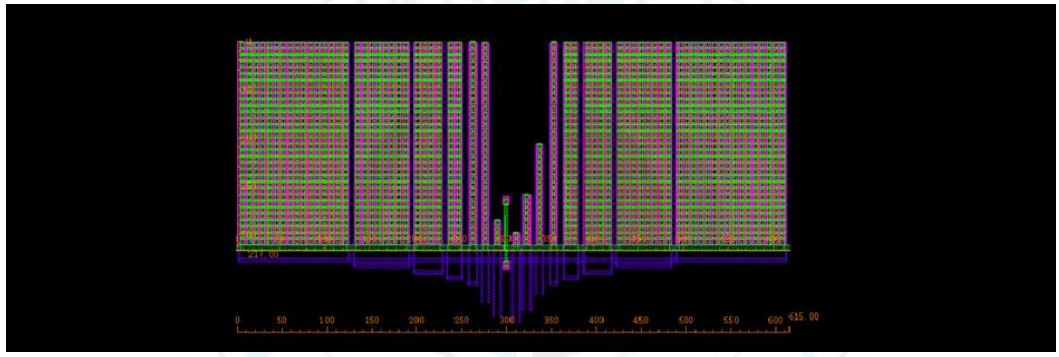
$$E_{ac} = \sum_{i=1}^{n} 2^{n+1-2i}\left(2^{i} - 1\right)CV_{ref}^{2} \tag{3.2}$$

$$E_{aw} = \sum_{i=1}^{n-1} 2^{(n-2-i)}CV_{ref}^{2} \tag{3.3}$$

Let's consider 12-bit SAR ADC. The general structure has the average switching energy consumption of $1023.5CV_{ref}^{2}$, expressed in Equation (3.2). The proposed ADC has average switching energy consumption of 457.3 $CV_{ref}^{2}$ by Equation (3.3). Therefore, the proposed ADC has power consumption saving effect of about 55%. Figure 3.6 shows layout of the capacitor array network stage. Figure 3.6(a) shows the general structure of the capacitor array network stage with the length of about 1113.40μm, but the proposed structure provides the length of 615μm as shown in Figure 3.6(b). Therefore, the proposed structure has an area reduction of about 45%.



(a) the general structure



(b) the proposed structure

**Figure 3.6 Layout of capacitor array network stage**

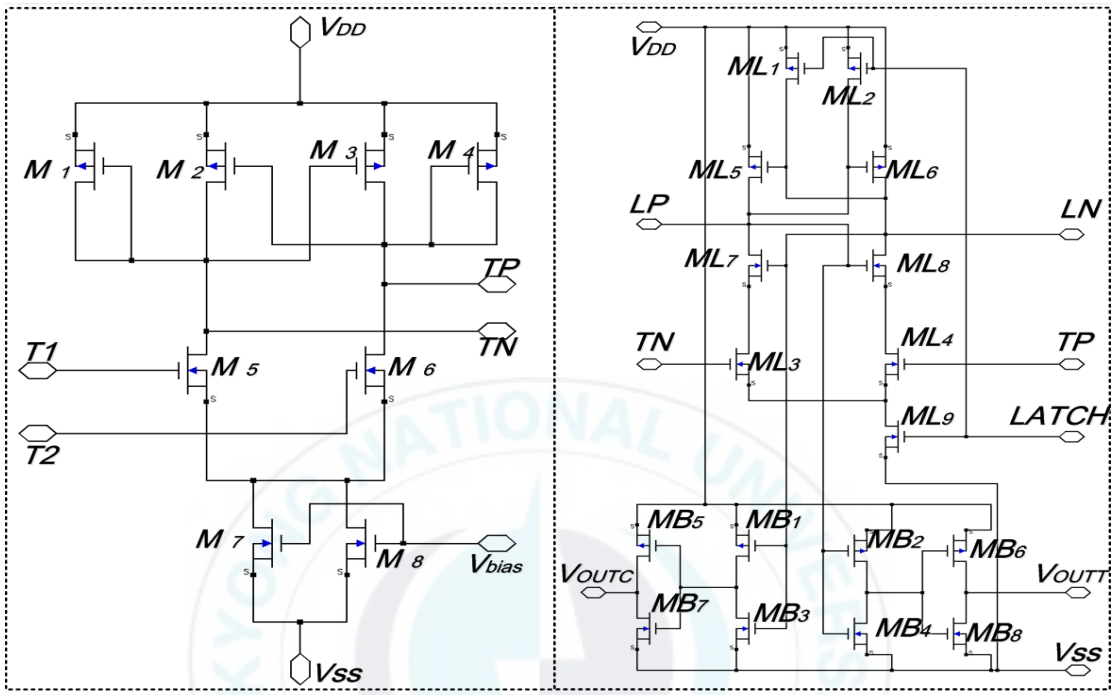
## 3.3 Comparator stage

The comparator stage requires pre-amplifier stage for high resolution of 12 bits to decrease latch offset and increase accuracy.

The comparator is a device that compares two voltage or currents and outputs a digital signal indicating which is larger. Figure 3.7 shows comparator stage with the latch and a buffer stage send compared result to the input of the SAR control logic stage and the DAC control logic stage. The output of the comparator stage holds successively information of 12 sets signal corresponding to the 12 bits from the MSB to LSB. Figure 3.7 is to propose a comparator stage it shows the pre-amplifier stage with the latch, and a buffer stage. Figure 3.7(a) shows circuit schematic of pre-amplifier with $M_1$~$M_8$ and Figure 3.7(b) shows the latch ($ML_1$ ~ $ML_9$) and the buffer stage ($MB_1$ ~ $MB_8$). The capacitor array network stage is applied to the pre-amplifier stage of the fully differential architecture through the *T1* and *T2* in Figure 3.7(a). Pre-amplifier amplifies the differential input voltage by a gain. *T1* and *T2* are applied to a bias voltage through the NMOS connected to the gate. TP and TN are amplified in the pre-amplifier, and output port is transferred to the latch stage. The differential output signal amplified by the pre-amplifier stage is passed through the latch and a buffer stage

to maximize the amplitude as shown in Figure 3.7(b). When the latch enters into equilibrium state enters (Reset), LN and LP wait the input signal for pre-charged $V_{DD.}$

$ML_9$ of the latch turns on 'High' status before clock 'Clks' of sample-and-hold stage is 'Low' status. At this time since $ML_1$ and $ML_2$ turn off, the latch detects the difference between the input signals of the gates of $ML_3$ and $ML_4$. This input difference is applied to the logic level on the LP and LN terminals through a feedback loop $M_5$ ~ $M_8$. These logic level signals are applied to comparator stage using $V_{OUTT}$ and $V_{OUTC}$ through the buffer consisting of $MB_1$ and $MB_9$. Since the buffer is connected in series with a latch, it provides a voltage level of comparator from the power supply voltage level to the ground level.




(a) Circuit schematic of preamp (b) Latch and buffer stage

**Figure 3.7 Comparator stage**

### 3.4 SAR control logic stage

SAR control logic stage receives from the comparison information signal from comparator stage, and it generates sequential control signals of 12 numbers using 12-bit digital signal. Sequential control signals created by the SAR control logic stage are transferred to the DAC control logic stage in the form of a clock signal. Figure 3.8 shows proposed SAR control logic stage. Output signals $V_{OUTT}$ and $V_{OUTC}$ of the comparator are

applied to the input of the SAR control logic stage. The clock '*Clks'* is realized by 'High' reset status of SAR logic in *'Low'* status (hold status). SAR logic output signal *'Clk_Out'* is used to the *'LATCH'* control clock of the comparator. SAR control logic output stage of $Clk_1$ ~ $Clk_{12}$ sample digital output code in association with the output signal of the comparator, as sequential control clock signal sampling and it is used as a control signal for carrying out switching process of the capacitor array. SAR control logic stage generates a control clock signal consisting of several gates and D flip-flop of 12 sets. In Figure 3.8 SAR control logic stage generates clock signal of 12 sets. Binary code of 12 bits generated using a clock signal of 12 starts to '100000000000'. Create when first comparator result is '1(High)' from SAR control logic stage in conjunction to DAC control logic stage, it provides '010000000000'. On the other hand, if the result of the comparator is '0(Low)', the output is '110000000000', and so the output repeated determines the binary code of the final 12 bits.

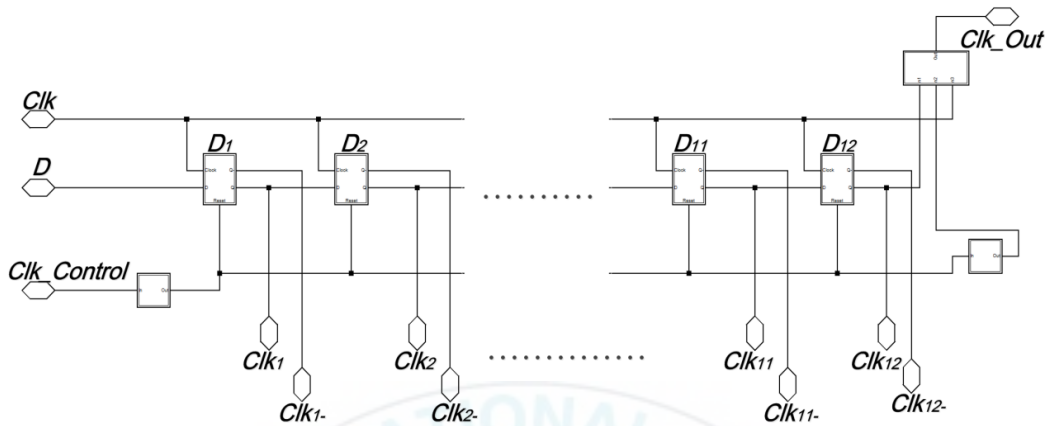



**Figure 3.8 SAR control logic stage**

## 3.5 DAC control logic stage

Figure 3.9 shows DAC control logic stage, and this stage is composed of D flip-flops, the delay buffer, the logic gate and the inverter. DAC control logic stage compares the information signal $V_{OUTT}$ with control clock signal $Clk_i$ *(i=1~12)*, since $V_{ref}$ and *GND* are connected to the input capacitor bottom plate composed of a total of four inputs. Output for the switching state at the bottom plate of the capacitor is $V_{pi}$, and *B_pi* port exports information bit which is sequentially determined by *V+* from capacitor top plate to the DAC stage.

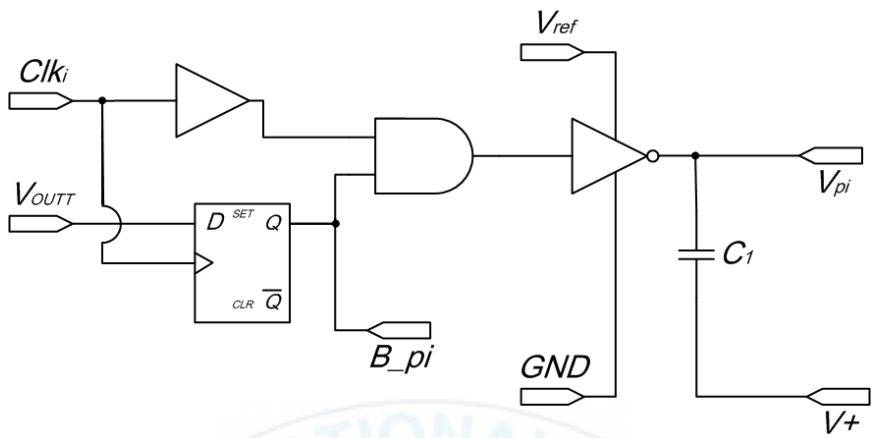



**Figure 3.9 DAC control logic stage**

In the DAC control logic stage delay buffer triggers between *Clki* and *AND* gate. In addition, to control the switching process of the stage capacitor array network it is designed using an AND gate and an inverter switch buffer.

### 3.6 DAC stage

The DAC stage under the control of the DAC control logic stage converts the digital signal into an analog signal, and then it sends signals to the input of the comparator. This output signal of the DAC is inserted to the input signal of the comparator to perform the successive approximation process.

Figure 3.10 shows DAC stage with 12 parallel control signal inputs from the DAC control logic stage. This stage contains one output port to send digital-to-analog signal through the capacitor array network. The proposed DAC is connected to the Op-amp for the capacitor array network consisting of 12 capacitors 10 with 12-bit resolution, as shown in Figure 3.

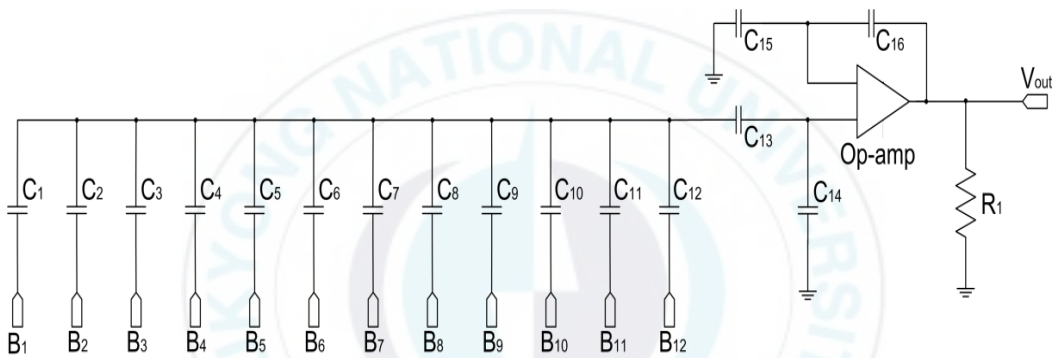



**Figure 3.10 DAC stage**

Figure 3.11 shows layout of DAC stage with capacitor array network. This layout is suitable for low-area applications because of recycling the blocks. It showed small area of 48μm × 39μm.

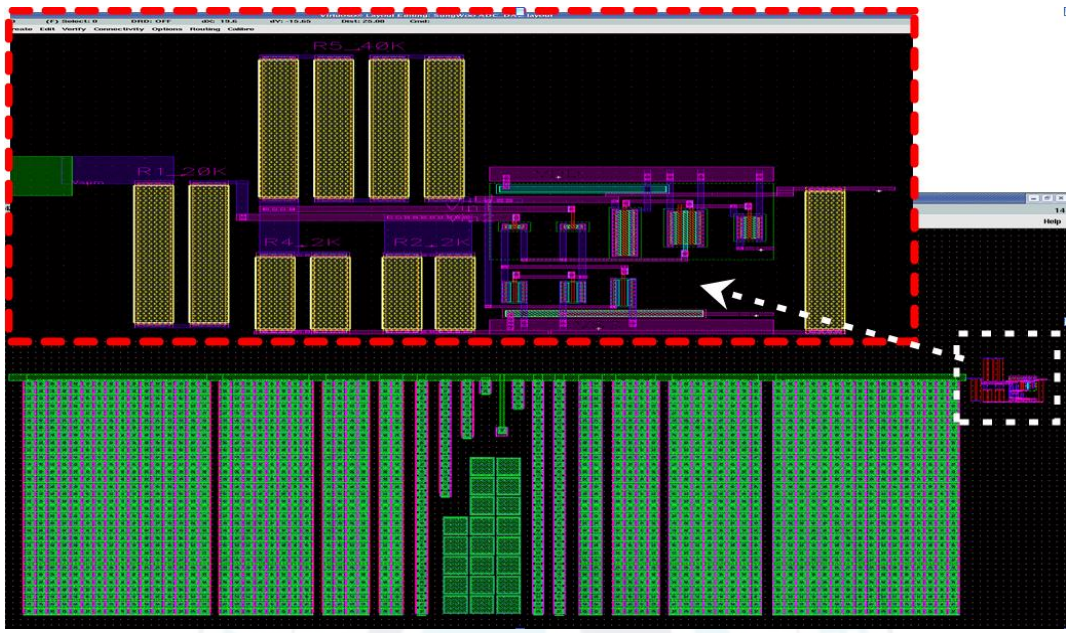



**Figure 3.11 DAC stage layout**

## 3.7 SAR ADC

Figure 3.12 shows total block diagram of SAR ADC, and Figure 3.13 shows layout of the SAR ADC. As shown in Figure 3.12 and Figure 3.13 it contains S/H stage, capacitor array stage, comparator stage, SAR control logic stage, DAC stage and DAC control logic stage. The proposed SAR ADC also showed small effective chip area of 0.54mm$^2$.

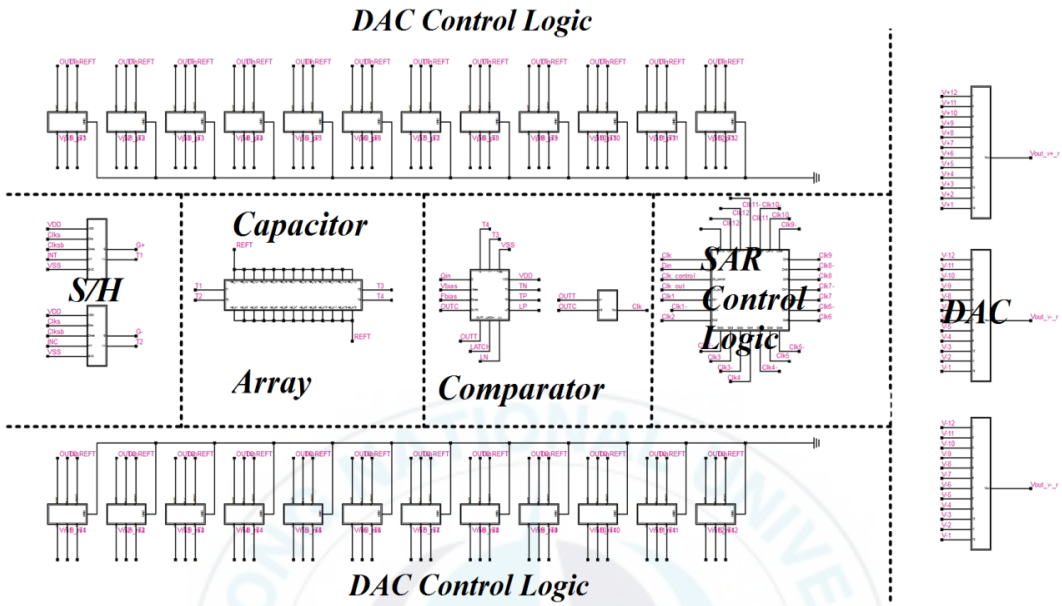



**Figure 3.12 Symbol block diagram of SAR ADC**

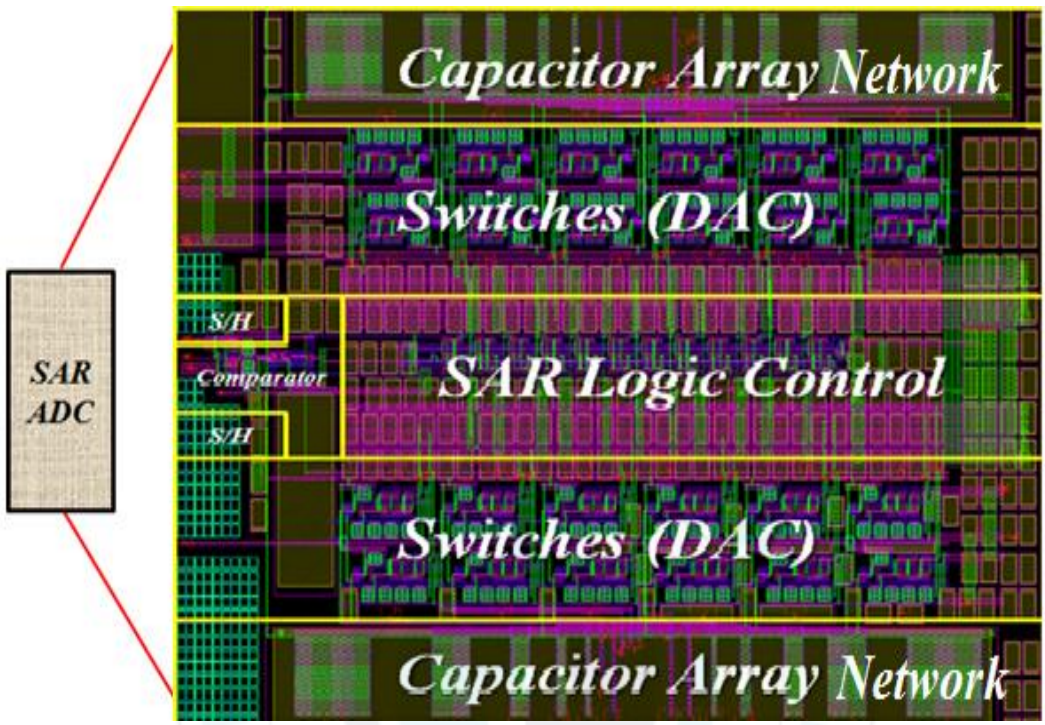


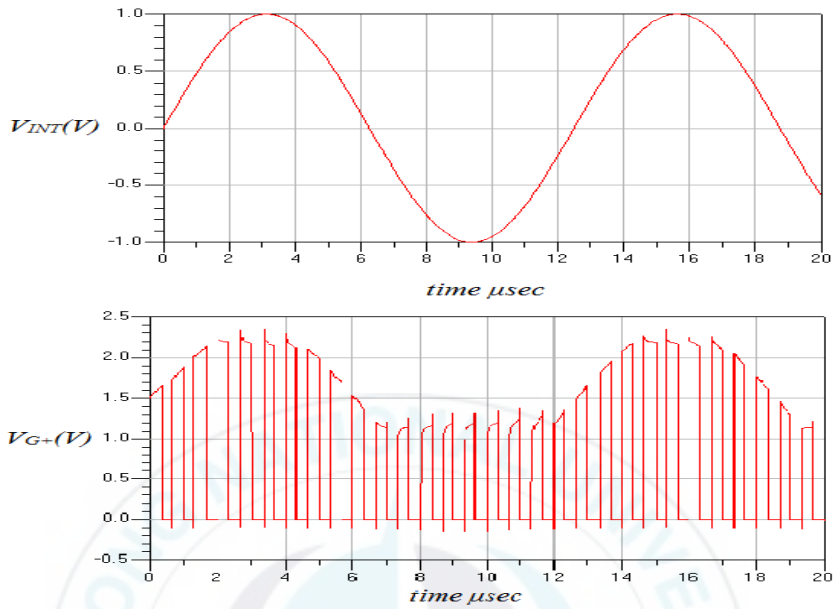

**Figure 3.13 Layout of SAR ADC**

# 4 Results and Analysis

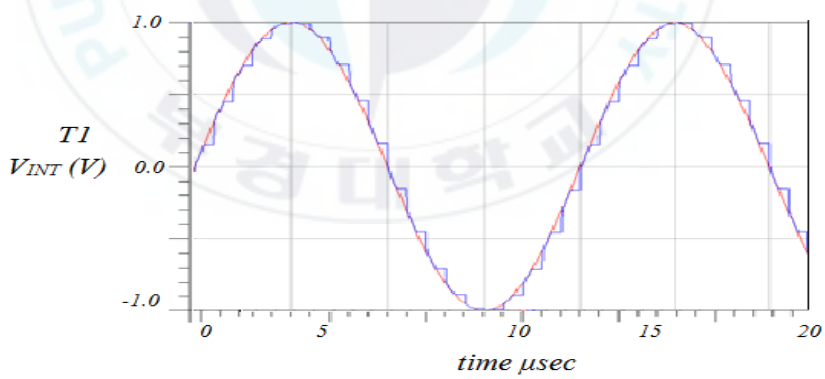
All simulations are performed by the power supply of 1.5V at room temperature of 25℃, and the ADC has the input bias voltage of 0.8V. It is also simulated at the input frequency of 80 kHz so that the output signal for the applications has the frequency of less than 80 kHz.

## 4.1 SAR ADC simulation results

Figure 4.1 shows simulation results of sample-and-hold stage. Figure 4.1(a) shows the simulation results for the sampling at the gate output $V_{G+}$ of $M_7$ of the sample-and-hold stage in Figure 3.2 as according to analog input voltage ($V_{INT}$). Figure 4.1(b) shows the simulation result for the relationship between the Input signal ($V_{INT}$) and sampling signal (*T1*). The results of analog input signal are sampled at a sampling rate of 1MSps. This output signal is transmitted to the input of the capacitor array network stage.



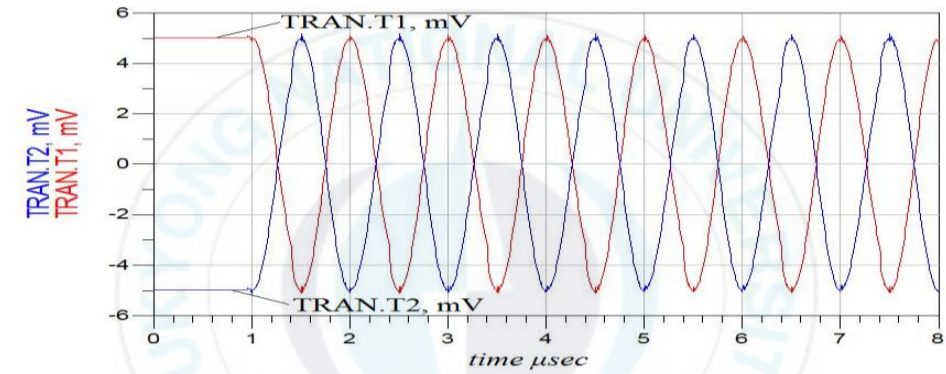

**(a) Input signal *($V_{INT}$)* and *$M_7$* gate signal.**



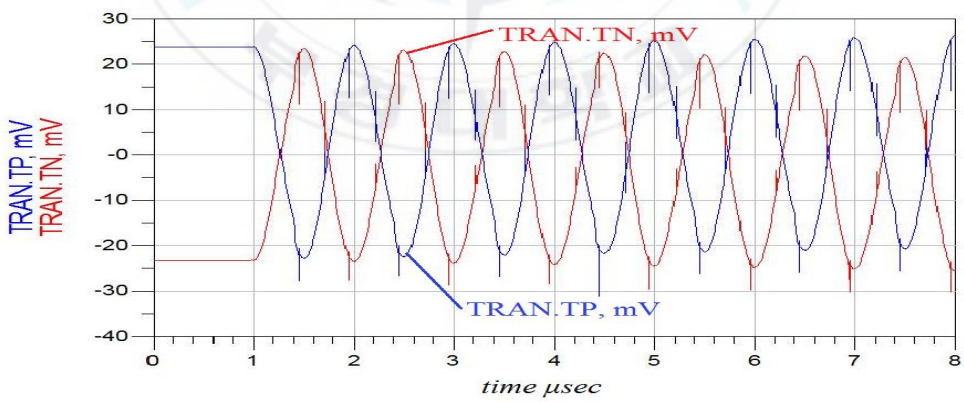

**(b) Input signal *($V_{INT}$)* and sampling signal (T1).**

**Figure 4.1 Simulation results of sample-and-hold stage**

Figure 4.2 shows the simulation result of the pre-amplifier stage of the comparator. Figure 4.2(a) is the input signal of the pre-amplifier stage. Small input signals of 5mV are applied to the pre-amplifier stage, and it is designed to amplify 5 times. As shown in Figure 4.2(b), the pre-amplifier stage showed output of approximately 25mV.




(a) Pre-amplifier input.

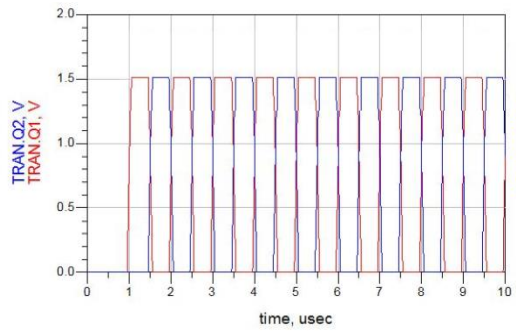



(b) Pre-amplifier output.

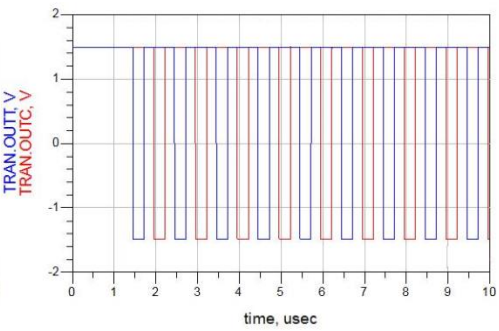
**Figure 4.2 Input(T1, T2) and output waveform(TN, TP) of pre-amplifier**

Figure 4.3 shows simulation results of the comparator. As shown in Figure 4.3(c) and Figure 4.3(e), when the latch clock is ‘Low’, *LN* and *LP* are pre-charged to ‘High’, and when the latch clock is ‘High’, the *LN* and *LP* ‘High’ or ‘Low’ are opposite to each other. Figure 4.3(d) and Figure 4.3(f) show the final output of the latch. When the output is changed as the change of the latch, so it provides $V_{OUTT}$ and $V_{OUTC}$ in ‘High’ status. These values are transmitted to SAR control logic stage is transmitted to the DAC control logic stage.

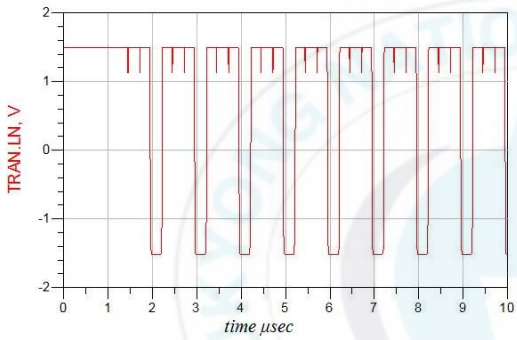
Figure 4.4 shows simulation result for clock timing diagram of the SAR control logic stage. As we can see in Figure 4.4, the reset signal *Clks* sequentially provides control signals of the 12 clock to control the capacitor array network. In addition, the ends of the control switch to the reference voltage of 12 clocks per one period are all ‘Low’.



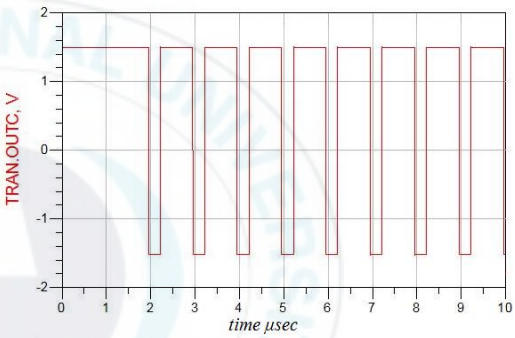

(a) Input clock



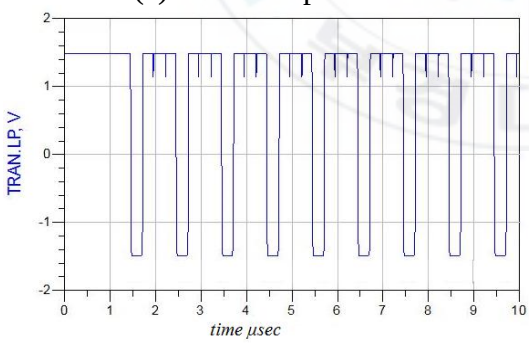

(b) Comparator output



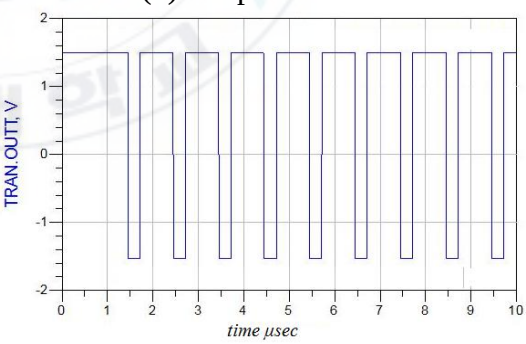

(c) Latch output LN




(d) Output OUTC




(e) Latch output LP




(f) Output OUTT

**Figure 4.3 Simulation result of comparator**

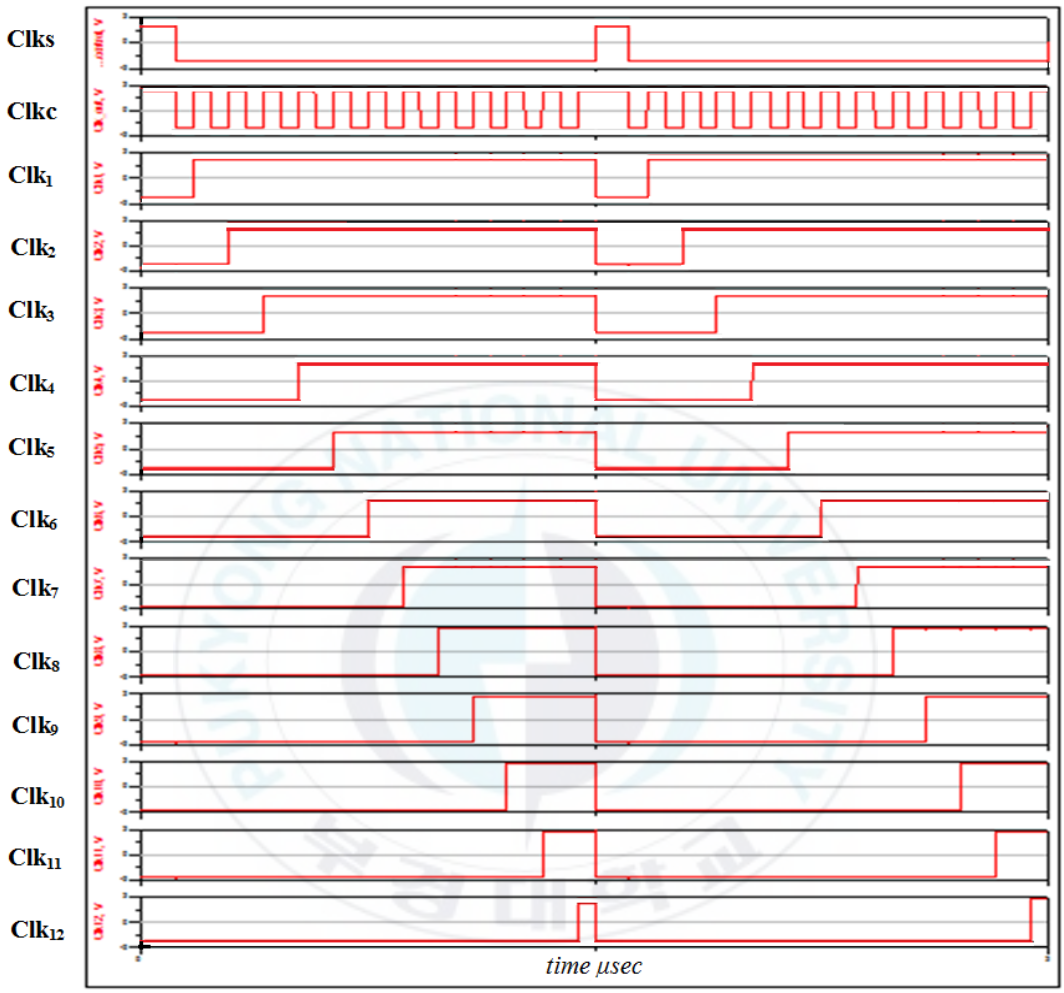
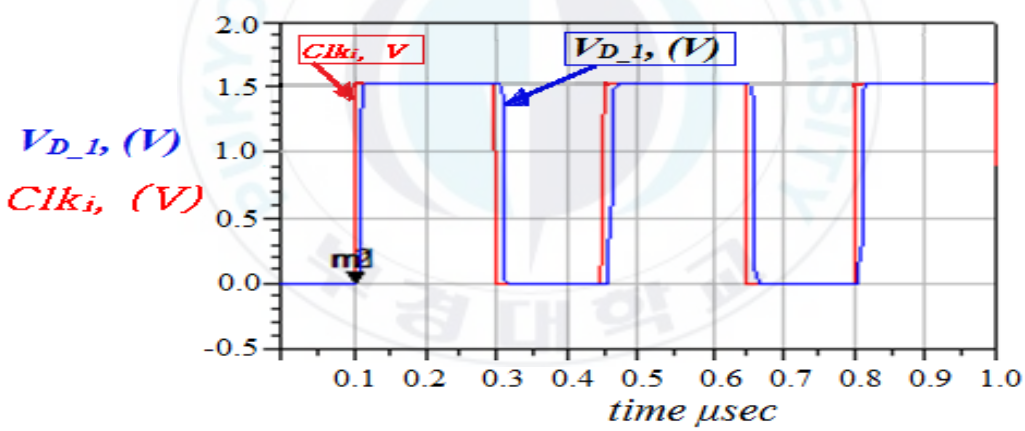
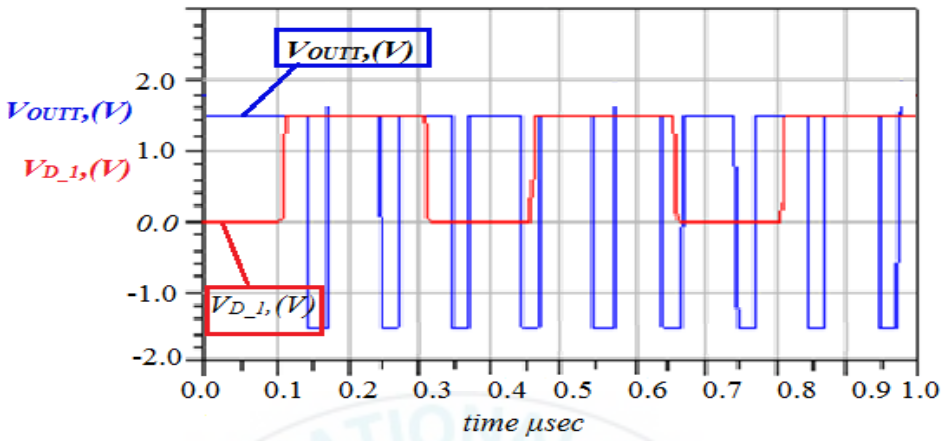



**Figure 4.4 Clock timing diagram of SAR control logic.**

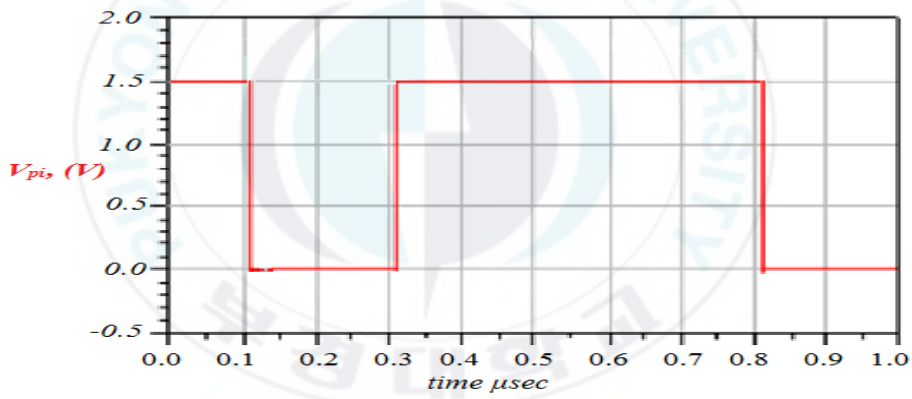
Figure 4.5 shows the simulation result of the DAC control logic stage. As shown in Figure 4.5(a) and Figure 4.5(b), D flip-flop is to sample the comparator output on the rising edge of the clock signal $Clk_i$. In this case, as shown in Figure 4.5(b) when comparator output $V_{OUTT}$ is 'High' the reference voltage $V_{ref}$ is switched to the ground. When the comparator output is 'Low', it is connected to the reference voltage. However, the falling edge of $Clk_i$ is always connected to the reference voltage as shown in Figure 4.5(c).




(a) D flip-flop signal and the clock signal



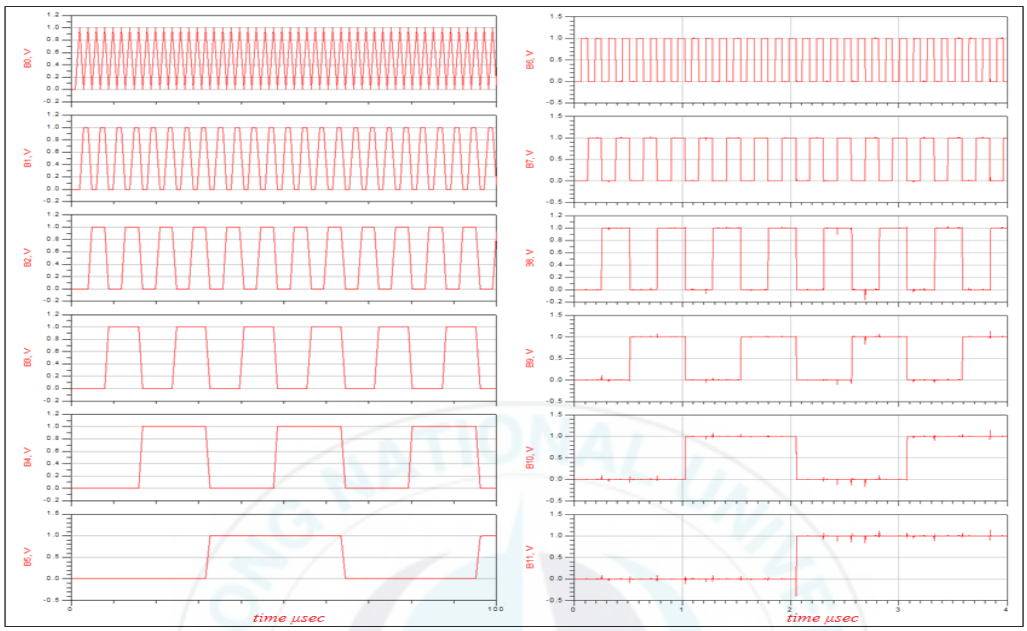

(b) D flip-flop signal and the comparator output signal



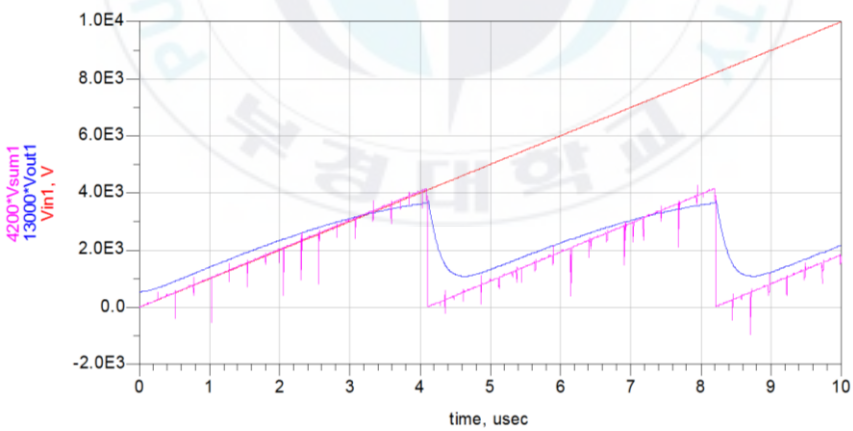

(c) Output signal of DAC control logic stage.

**Figure 4.5 Simulation results of DAC control logic**

Figure 4.6 shows the simulation result of the 12-bit DAC stage. After the ramp input signal is converted into digital signal of 12 bits as shown in Figure 4.6(a), the DAC stage simulates the process to be re-converted into a ramp signal as shown in Figure 4.6(b). As can be seen from Figure 4.6, the digital input of 12-bit through DAC stage is converted into the ramp waveform.




(a) 12-bit input signal of DAC stage




(b) Ramp input signal and output signal of DAC stage.

**Figure 4.6 (a) and (b) Simulation results of 12-bit DAC stage**

## 4.2 SAR ADC implementation and performance evaluation

Figure 4.7 shows the result of Fast Fourier Transform (FFT) for the input signal of 80 kHz. The proposed ADC showed high signal-to-noise distortion ratio (SNDR) of 71.18dB, and excellent effective number of bit (ENOB) of 11.53-bit as compared to current research results.

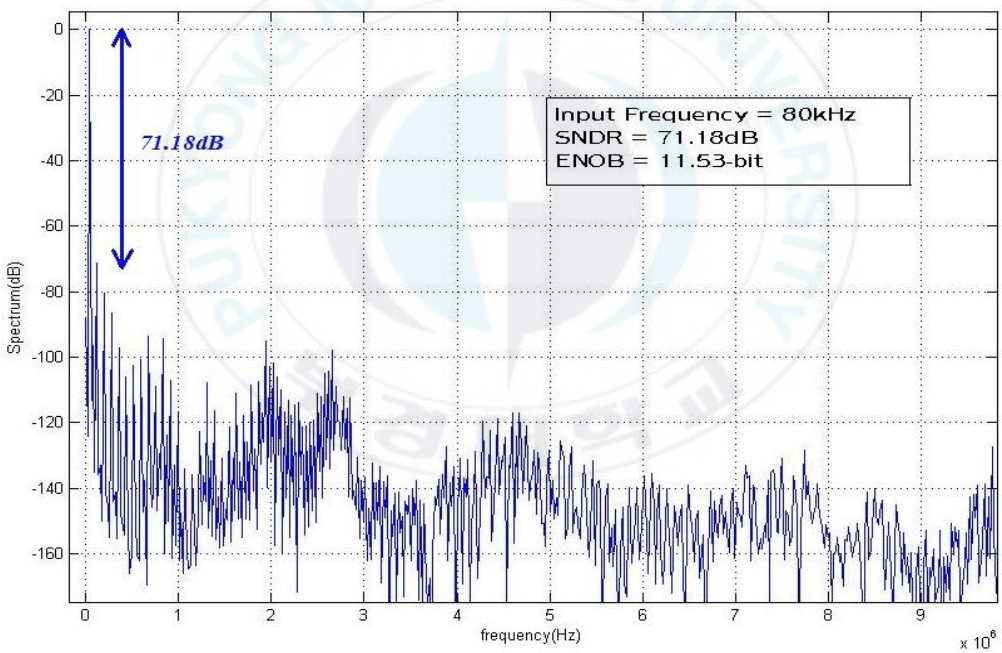



**Figure 4.7 FFT result of SAR ADC**

Table 4.1 compares the results of proposed SAR ADC as compared to current research results. The effective number of bits (ENOB) and signal-to-noise distortion ratio (SNDR) represent excellent characteristics to larger values and, the power consumption and the chip area represent more excellent properties to smaller values. As we can see from Table 4.1, the proposed SAR ADC showed very low power consumption of 1.95mW in a supply voltage of 1.5V and small chip area of only 0.54mm$^2$.

Table 4.1 Summary and comparison of SAR ADC performance

| | In this work | [9] | [10] | [11] | [12] |
|---|---|---|---|---|---|
| Performances | SAR | SAR | SAR | SAR | SAR |
| Technology(μm) | 0.18 | 0.6 | 0.18 | 0.18 | 0.18 |
| Conversion Speed(Sps) | 1M | 1M | 1M | 1M | 1M |
| ENOB(bit) | 11.53 | 11.3 | 10.5 | 11.34 | 10.8 |
| SNDR(dB) | 71.18 | 69.79 | 64.97 | 70.03 | 66.78 |
| Power Consumption(mW) | 1.95 | 15 | 2 | 3.24 | 1.5 |
| Supply Voltage(V) | 1.5 | 3.0-5.5 | 1.8 | 1.8 | 1.8 |
| Effective chip area(mm$^2$) | 0.54 | 1.5 | 1 | 0.56 | 0.64 |
| Resolution(bit) | 12 | 12 | 12 | 12 | 12 |

# 5 Conclusions

In this thesis, a 12-bit successive approximation register type 1MSps analog-to-digital converter is proposed. It contained sample-and-hold stage, capacitor array, SAR control logic stage, DAC stage, and DAC control logic stage. This SAR ADC is designed to have performance of 12-bit resolution and.

The SAR ADC was verified by simulating the performance using the Advanced Design System (ADS) tool, and the Magnachip/SK Hynix's 1-Poly 6-Metal 0.18μm CMOS process was used for Cadence's Virtuoso layout tools.

The proposed circuit in this thesis showed high signal-to-noise distortion ratio (SNDR) of 71.18dB, and excellent effective number of bit (ENOB) 11.53-bit as compared to conventional research results. The designed circuit also showed very low power consumption of 1.95mW, in a supply voltage of 1.5V and small chip area of 0.54mm$^2$.

# References

[1] M. U. Seong, Murod Kurbanov and J. Y. Ryu, “A 12bit 1MSps SAR ADC for System-on-Chip”, Proceedings of Conference on Information and Communication Engineering, June 2016.

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**[Appendix]**

## Publication Paper List

### (1) Journal

| Paper Title | Date | Journal Title |
|---|---|---|
| 24GHz CMOS Power Amplifier for Automotive Radar | January 2017 | International Journal of Control and Automation (**SCOPUS**) |
| Design of Low-Power 24GHz Voltage-Controlled Oscillator | December 2016 | AETA (**SCOPUS**) |
| A 12-bit 1MSps SAR ADC with High ENOB | August 2016 | International Journal of Applied Engineering Research (**SCOPUS**) |

### (2) Conference

| Paper Title | Date | Conference Title |
|---|---|---|
| Design of Low-Power 24GHz Voltage-Controlled Oscillator | December 2016 | The International Conference on Advanced Engineering-Theory and Applications 2016 |
| Design of Digital FIR Filters for Noise Cancellation | October 2016 | Proceedings of Conference on Information and Communication Engineering |
| Low-Power 24-GHz CMOS Low Noise Amplifier | October 2016 | Proceedings of Conference on Information and Communication Engineering |
| A low power 12-bit 1MSps SAR ADC with capacitor array network | October 2016 | 2016 년도 한국멀티미디어학회 추계학술발표대회 논문집 제 19 권 2 호 |
| An Ultra-Low Power 24GHz CMOS LC VCO | October 2016 | 2016 년도 한국멀티미디어학회 추계학술발표대회 논문집 |

| | | |
|---|---|---|
| | | 제 19 권 2 호 |
| 12-bit 1MSps SAR ADC for System-on-Chip | June 2016 | 대한전자공학회 전자·통신 학술대회 |
| Automotive Radar Frontend Circuit in 0.13μm CMOS | June 2016 | 대한전자공학회 전자·통신 학술대회 |
| Design of a Low Area 12-bit SAR ADC using MOS Capacitor | June 2016 | 대한전자공학회 전자·통신 학술대회 |
| Development automobile engine measurement device using a laser and a CCD linear sensor. | June 2016 | 대한전자공학회 전자·통신 학술대회 |
| FPGA implementation of programmable FIR/IIR filter | June 2016 | International Conference on Future Information and Communication Engineering |
| 5.25-GHz BiCMOS Low Noise Amplifier | May 2016 | Proceedings of Conference on Information and Communication Engineering |
| Design of Bias Circuit for GHz BiCMOS Low Noise Amplifier | May 2016 | Proceedings of Conference on Information and Communication Engineering |
| High Gain 24-GHz CMOS Low Noise Amplifier | May 2016 | Proceedings of Conference on Information and Communication Engineering |
| Development of DPSD(Digital Position Scanning Device) Using Laser and Linear CCD Sensor | December 2015 | 한국통신학회 학술심포지움 논문집 |
| The Low Area 12-bit SAR ADC using CMOS Process | December 2015 | 한국통신학회 학술심포지움 논문집 |
| Development of Low-Power CMOS Programmable Gain Amplifier | October 2015 | ISAE 2015 International Symposium on Advanced Engineering |
| The High-Linearity CMOS LNA using Modified DS Linearization Technique | October 2015 | ISAE 2015 International Symposium on Advanced Engineering |
| Fabrication of a Low-Cost Wafer-Level Packaging for RF Devices | October 2015 | ISAE 2015 International Symposium on Advanced Engineering |
| Design of power Amplifier for 24- | October 2015 | ISAE 2015 |

| | | |
|---|---|---|
| Applications | | International Symposium on Advanced Engineering |
| Design of Low-Power Voltage-Controlled Oscillator for 24-GHz Applications | October 2015 | Proceedings of Conference on Information and Communication Engineering |
| Implementation of Vehicle Collision Avoidance Algorithm for Automotive Radar Sensor | October 2015 | Proceedings of Conference on Information and Communication Engineering |
| The Low Area 12-bit SAR ADC | October 2015 | Proceedings of Conference on Information and Communication Engineering |
| 77-GHz 저전력 전압제어발진기 설계 | October 2015 | 2015 한국정보기술학회 ICT 논문 경진 대회 논문집 |
| Design of 24-GHz/77-GHz Dual Band CMOS Low Noise Amplifier | May 2015 | Proceedings of Conference on Information and Communication Engineering |
| Design of 77-GHz CMOS Power Amplifier | May 2015 | Proceedings of Conference on Information and Communication Engineering |

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Finally, I wish to thank my parents in Samarkand Uzbekistan for allowing me to come to Busan South Korea. They provided me with support and encouragement.

Murod Kurbanov

February, 2017, Pukyong National University, Busan

**Keywords**

ADC-Analog to Digital Conversion

DAC-Digital to Analog Conversion

SAR-Successive Approximation Register

SoC-System on Chip

CMOS- Complementary Metal Oxide Semiconductor

ENOB-Effective Number of Bits

SNDR-Signal to Noise Distortion Re Ratio

SNR-Signal to Noise Ratio

S/H-Sample and Hold

INL-Integral non-Linearity

DNL-Differential non-Linearity

LSB- Less Significant Bits

MSB-Most Significant Bits

MSps-Mega Sampling per second

(Σ-Δ)-Sigma-Delta

FFT-Fast Fourier Transform