Thesis for the Degree of Master of Engineering

A jitter characteristic improved PLL with RC time constant circuit

by

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February 24, 2017

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(저항-커패시턴스 시정수 회로를 이용하여 지터 특성을 개선한 위상고정루프)

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A dissertation

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요　　약

본 논문은 RC 시정수 회로를 이용하여 지터 특성을 개선한 위상고정루프의 구조를 제안하였다. RC 시정수 회로에서는 루프 필터 전압이 작은 시정수와 큰 시정수 값을 가지는 회로를 통과하여 비교기로 전달된다. 작은 시정수 값을 가지는 회로를 지나는 신호는 거의 루프 필터 출력 전압과 같은 값을 가진다. 큰 시정수 값을 가지는 회로를 지나는 신호는 루프 필터 출력 전압의 평균값을 가지며, 비교기회로에서 기준 신호 역할을 한다. 비교기의 출력 신호는 루프 필터에 전류를 공급하는 보조 전하펌프를 제어한다. 루프 필터 출력 전압이 상승하면 보조 전하펌프는 루프 필터에서 전류를 방전시켜 루프 필터 출력 전압이 하강하게 하고, 또는 루프 필터 출력 전압이 하강하면 보조 전하펌프는 루프 필터에서 전류를 충전시켜 루프 필터 출력 전압이 상승하게 한다. 이런 부궤환 루프는 필터 출력 전압 변동 폭을 줄여서 지터 크기를 감소시켜준다.

Ⅰ. Introduction

In many communications and control applications like clock recovery and frequency synthesis, phase-locked loop (PLL) circuits are widely used. With the ever increasing data rates, phase noise and jitter have become critical specifications of modern PLL design[1]. The main cause of frequent phase noise and jitter on the PLL is because of instability of the voltage controlled oscillator (VCO). VCO is one of the most sensitive circuits affected by external variables such as temperature, supply voltage and process variation. Since the VCO outputs constant frequency component according to the LPF voltage at its output, voltage fluctuation of the LPF causes irregular pulse sequence of frequency on the VCO. Therefore, voltage fluctuation of the LPF in a locked state makes countless phase noise and jitter on the VCO output[2].

Recently, lots of various PLL structures have been proposed and researched to reduce phase noise. The improvement on the noise characteristics was made by controlling adaptive two-bandwidth with the VCO[3]. On the other hand, two-symmetrical loop complicated the circuit and enlarged the size of a chip. Using low gain VCO design and analog band-selection loop is another way to improve the phase noise[4, 5]. This uses dual loop and switched-capacitor networks to ensure wide-area frequency, but it slows the speed of phase locking

time. Reference[6] presents the linear technique to reduce phase noise arose from the dead zone of PFD or current mismatching of CP. However, the improvement of the CP's nonlinearity produced more noise as the transistor's operation time extended. The relocation of VCO output makes PLL very sensitive to reference frequency noise[7]. This approach has limitations of the effective phase noise suppression on the overall PLL. In order to reduce jitter, active loop filter (ALF)[8] and two ring-oscillation VCO control techniques[9] are presented. By using the LDO-regulator, the DC supply voltage is increased as well as the noise due to the output ripple voltage.

In this paper, voltage fluctuations in LPF is minimized through the RC time constant comparator and the auxiliary charge pump. With such stabilized voltage of VCO, stable output frequency is produced. As a result, phase noise and jitter property of on the total PLL circuit can be improved.

Ⅱ. Basic principle of phase locked loop.

2.1 The structure and principle of PLL

Numerous ways of implementing frequency synthesis or clock signal generator have been proposed. One of them being a PLL (Phase-locked loop) has gained popularity, due to its advantages such as low phase noise and low spur distribution. A PLL is a circuit to make a signal, which has the same frequency and phase with a reference signal. The typical characteristics of PLL performance are phase noise, phase locking time, and spur. All of these are affected by the PLL bandwidth. The PLL bandwidth has the tradeoff relation with the phase locking time and noise; when the PLL bandwidth becomes wider, the phase locking time shortens with worse noise characteristics, and when it becomes narrower, the opposite effects emerge. Also, the bandwidth depends on the reference frequency which is permitted by PLL. The PLL this paper deals with is Charge Pump PLL and the basic block diagram of it is shown in Figure 2.1.

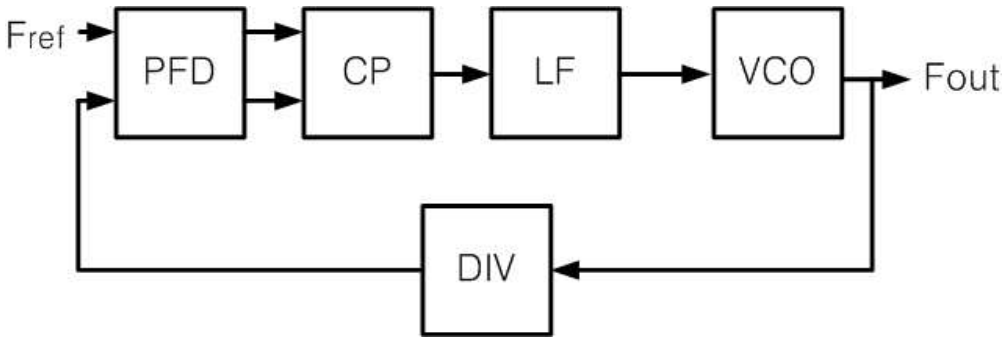


Figure 2.1 Block diagram of the basic phase locked loop.

PLL consists of PFD (Phase Frequency Detector), CP (Charge Pump), LF (Loop Filter), VCO (Voltage Controlled Oscillator) and Div (Divider). Under normal conditions of the PLL, PFD attempts to compare the external reference phase frequency signal and the frequency signal produced by the VCO, which consequently regulates the CP by using the signal that demonstrates the pulse of the difference.

The CP charges or discharges the LPF's capacitor through the current, which has the proportional pulse width of the input signal. Such action generates VCO control voltage that evens out the VCO output phase·frequency signal and reference phase·frequency signal. Although the process of PLL is nonlinear while unlocked, it can be designed as a linear PLL model after it is locked. Figure 2.2 shows PLL linear model at its locked state, and the transfer function is given below (2-1).

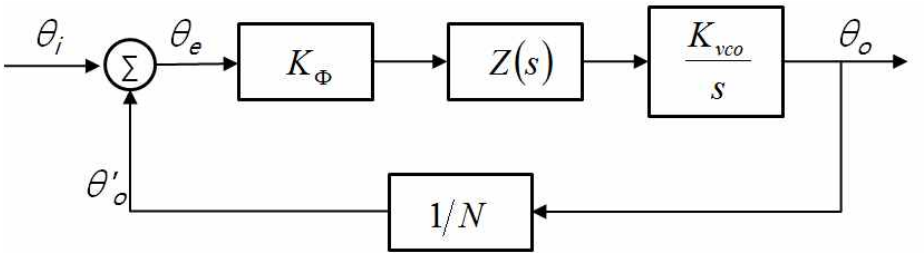


Figure 2.2 The linear PLL model in the locked state.

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_\Phi \cdot Z(s) \cdot \frac{K_{VCO}}{s}}{1 + \frac{1}{N} \cdot K_\Phi \cdot Z(s) \cdot \frac{K_{VCO}}{s}} \tag{2-1}$$

2.2 Performance of the basic blocks

2.2.1 Phase frequency detector (PFD)

The PFD is generally used to compare the phase of two clocks. Static skew, bang-bang jitter and others are determined by the characteristics of PFD. The D Flip-Flop, which is commonly used as the PFD, may increase jitter due to the existence of uncertain region according to the set/hold time. In addition, one of the biggest disadvantages it has is the possibility of bang-bang jitter because the D Flip-Flop can only detect the positive (+) or negative (-) on the phase error.

Today, the 3-state PFD structure, which is able to detect the phase and frequency simultaneously, are widely used. Figure 2.3 shows the 3-state PFD structure.

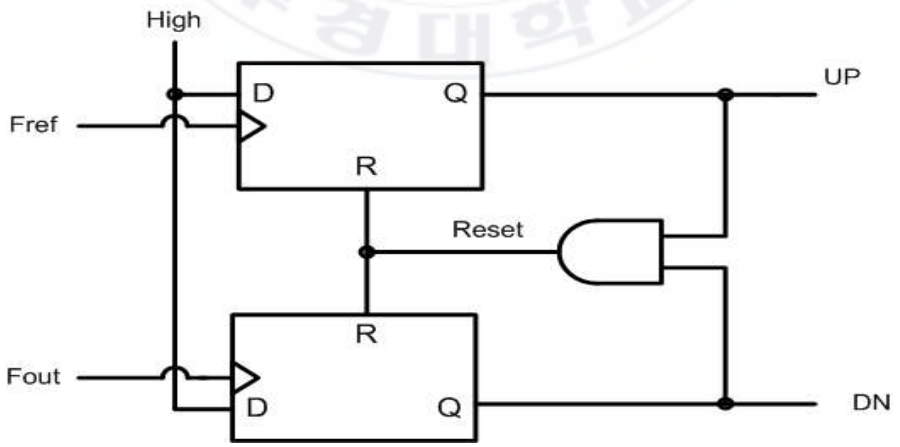


Figure 2.3 Basic structure of the PFD

The 3-state PFD is comprised of two D Flip-Flop and one AND gate. An edge-triggered sequence circuit, which strictly follows the implementing condition of reference frequency and VCO output frequency, shows no significant relationship with duty ratio of the two input signals. The phase diagram of the 3-state PFD is shown in Figure 2.4. The PFD generates a pulse width that is proportional to the phase difference between VCO output signal and reference signal, and sends out UP or DN pulse signal depending on the speed of two input signals.

For example, if reference signal is faster than VCO output signal, PFD outputs UP signal, which corresponds to the difference in pulse width. On the other hand, if reference signal is slower than VCO output signal, it outputs DN signal, which also corresponds to the difference in pulse width.

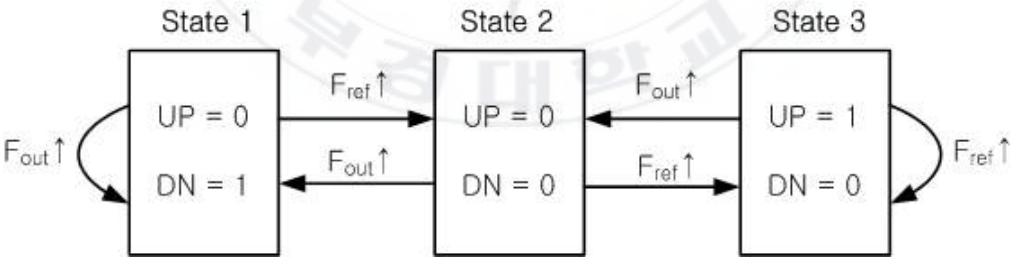


Figure 2.4 The Phase diagram of the PFD

The output UP signal of PFD increases the voltage of the LPF capacitor through the CP. The output DN signal of PFD decreases the voltage of the LPF capacitor through the same way.

When reference signal and the VCO output signal are the same, UP and DN signals of the PFD disappear, which stops the additional charge or discharge of the CP. Since the current stability of the CP prevents the LPF capacitor from producing additional fluctuation, the input control voltage of the VCO always keeps its constant value. In reality, however, some kind of reset pulses are generated by the reset time of the D Flip-Flop.

If the phase difference between the two input signals which are inputted at the PFD is $\triangle\Theta$, The PFD will generate the period of $1/f_{PFD}$ and the pulse(duration) of $|\Delta\theta|/\omega_{PFD}(=2\pi f_{PFD})$. If the current of CP is I_p, it will transfer the current of $I_p\Delta\theta/2\pi$ per period to the LPF. The LPF changes the transferred current to voltage. This process is shown in the equation as follows (2-2).

$$V_{cont}(s) = \frac{1}{2\pi} \cdot I_p \cdot G_{LF}(s) \cdot \Delta\theta(s) \qquad (2\text{-}2)$$

In the above expression, V_{cont} and G_{LF} stand for output voltage of the LPF and the transfer function of the LPF.

2.2.2 Charge pump (CP) and loop filter(LF).

Figure 2.5 shows the structure of the CP (Charge Pump) and LF (Loop Filter) at PLL. The CP charges or discharges current with UP or DN signals from the PFD. The CP is comprised of current source, sink and switches that turn current source on or off through controlling UP, DN signals. Current supply controlled by UP and DN of the CP does play a critical role in determining the PLL performance because it affects jitter of the PLL output frequency.

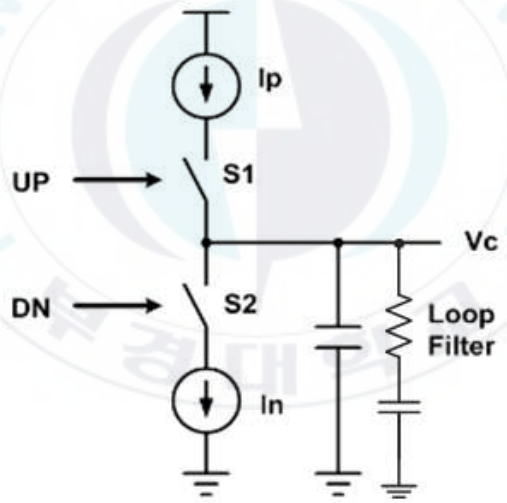


Figure 2.5 The charge pump and
the loop filter.

(As it can be seen on the CP,) When the UP signal gives 'high,' the S_1 switch on the CP turns on and I_P current flows into the LPF. As the LPF capacitor charges, VCO's input control voltage V_C gradually

increases. In contrast, When the DN signal gives 'high', the S_2 switch on the CP turns on and I_N current flows from the LPF out to the ground, which discharges the LPF capacitor's electric charge. And ultimately decreases the VCO's input control voltage V_C.

Since the S_1 and S_2 switches are simultaneously turned on during the reset at the locked state of the phase, there is no charging or discharging on the capacitor of the LPF. Therefore, the input control voltage of the VCO has steady and constant value.

As the switching element on the CP, P-type MOSFET is used for S_1 and N-type MOSFET for S_2. When PLL is at its locked state, the amount of CP's current I_P, I_N have to be the same. However, the current mismatch occurs because of the difference in movement of P-type and N-type MOSFET switches, the different 'turn on' time of switches that are generated by the output of the PFD and clock feedthrough of MOSFET switch and the charge injection. Current mismatch, which is generated by these elements, causes the fluctuation of the input control voltage and results in larger jitter.

2.2.3 Voltage controlled oscillator (VCO)

The VCO generates frequency, which is proportional to the input voltage, and its expression is given below (2-3).

$$\omega_{out} = \omega_{free} + K_{vco} \cdot V_{cont} \tag{2-3}$$

In the above expression, the ω_{free} stand for free running frequency of the VCO without V_{cont} and K_{VCO} stands for the gain of the VCO. The calculation of the transfer function of the VCO from the above expression is shown in (2-4).

$$\Phi_{out}(s) = \frac{1}{s} \cdot K_{vco} \cdot V_{cont} \tag{2-4}$$

2.2.4 Divider

In order to compare output frequency with input reference frequency, the output frequency of VCO cannot be used as is, so the frequency divider is used. Depending on the characteristics of its use, the frequency divider is classified into two ways: constant or fractional rate.

2.3 Linear analysis of the charge pump PLL

By analyzing the typical performance of the loop at s-domain, the open-loop transfer function and the closed-loop transfer function can be expressed as (2-5) and (2-6).

$$H_{open} = K_{PFD} \cdot \frac{K_{VCO}}{s} \cdot G_{LF}(s) \tag{2-5}$$

$$H_{closed}(s) = \frac{K_{PFD} \cdot K_{VCO} \cdot G_{LF}(s)}{s + K_{PFD} \cdot K_{VCO} \cdot G_{LF}(s)} \tag{2-6}$$

Based on the above equation, the calculations of the open-loop transfer function of the PLL and that of the closed-loop are shown as (2-7) and (2-8).

$$\frac{\theta_o(s)}{\Delta\theta(s)} = \frac{1}{2\pi} \cdot I_p \cdot G_{LF}(s) \cdot \frac{K_{VCO}}{s} \tag{2-7}$$

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{K_{VCO}}{s} \cdot \frac{I_p}{2\pi} \cdot G_{LF}(s)}{1 + \frac{K_{VCO}}{s} \cdot \frac{I_p}{2\pi} \cdot G_{LF}(s)} \tag{2-8}$$

$G_{LF}(s)$ presents the transfer function of the loop filter, and a low pass filter is used.

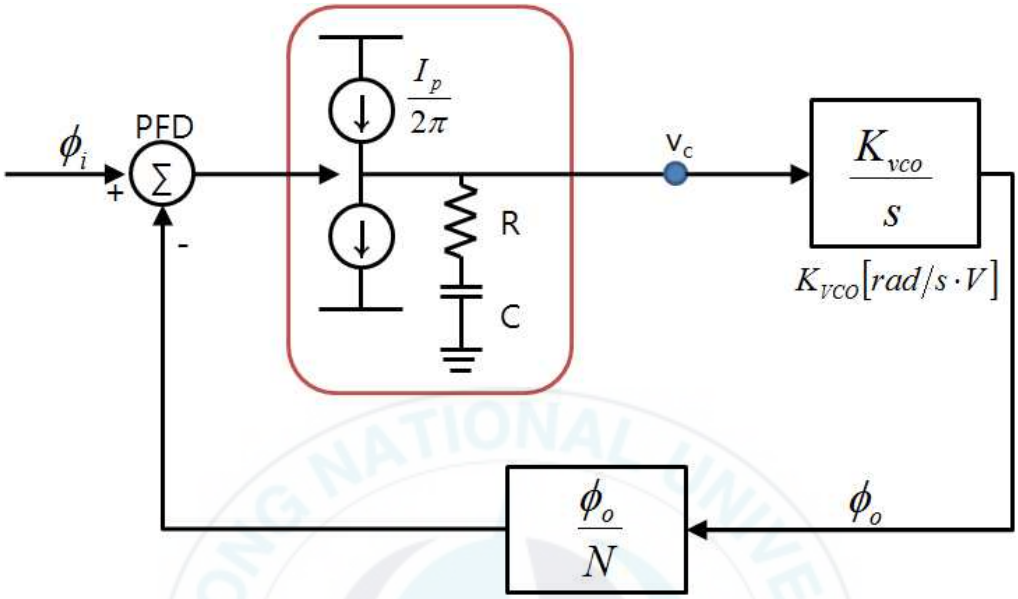


Figure 2.6 The second-order structure CP PLL.

Figure 2.6 shows the basic PLL that has the first-order transfer function on the LPF and VCO. By calculating according to the function in (2-7), the outcome turns out to be what is shown in (2-9).

$$\frac{\phi_o}{\phi_i} = \frac{N\left(\frac{1}{N}\cdot\frac{I_p}{2\pi}\cdot R\cdot K_{VCO}\cdot s + \frac{1}{N}\cdot\frac{I_p}{2\pi}\cdot K_{VCO}\cdot\frac{1}{C}\right)}{s^2 + s\cdot\frac{1}{N}\cdot\frac{I_p}{2\pi}\cdot R\cdot K_{VCO} + \frac{1}{N}\cdot\frac{I_p}{2\pi}\cdot K_{VCO}\cdot\frac{1}{C}} \qquad (2\text{-}9)$$

$$= \frac{2\zeta\omega_n\cdot s + \omega_n^2}{s^2 + 2\zeta\omega_n\cdot s + \omega_n^2}$$

As the figure 2.6 shows, the PLL structure is rarely used because the

resistor component shows a rapid change of the V_C through I_P, which makes unexpected output signal (spur) and other problems.

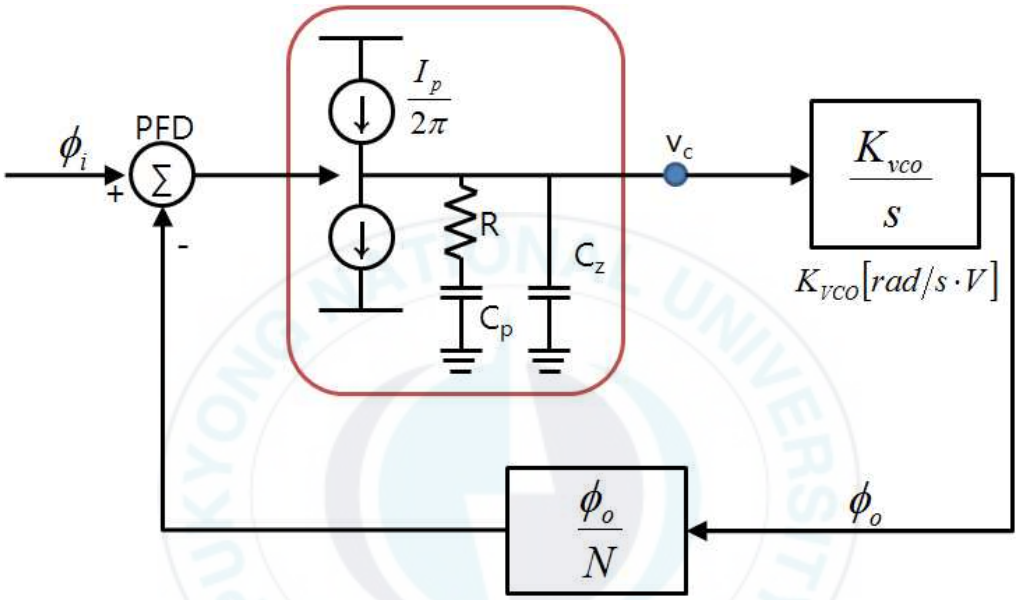


Figure 2.7 The third-order CP PLL.

In the case of using the third-order loop consisted of the second-order LPF, the PLL can be stabilized and reduce spur. According to the transfer function of the second-order LPF, where two poles are located at the origin point and another pole and zero determine the phase margin that is associated with loop stability and bandwidth. Figure 2.8 shows the 2-order LPF.

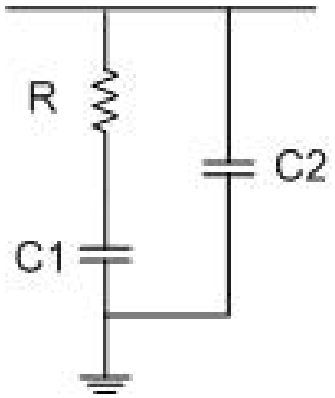


Figure 2.8 The second-order low pass filter.

The open-loop and the closed-loop transfer function of the total PLL in the 2-order LPF is given below.

$$H_{open}(s) = \frac{1}{2\pi} \cdot I_p \cdot \frac{1 + s \cdot R \cdot C_1}{s(C_1 + C_2) + s^2 \cdot R \cdot C_1 \cdot C_2} \cdot \frac{K_{VCO}}{s} \tag{2-10}$$

$$H_{closed}(s) = \frac{K_{VCO} \cdot I_p \cdot (1 + s \cdot R \cdot C_1)}{K_{VCO} \cdot I_p + K_{VCO} \cdot I_p \cdot R \cdot C_1 \cdot s + 2\pi(C_1 + C_2)s^2 + 2\pi \cdot R \cdot C_1 \cdot C_2 \cdot s^3} \tag{2-11}$$

The above (2-10) has three poles and one zero. The two poles are located at the origin point, the third pole is at $\frac{C_1 + C_2}{R \cdot C_1 \cdot C_2}$ and one zero is $\frac{1}{R \cdot C_1}$. Figure 2.9 shows the bode phase plot of the open-loop transfer function (2-10).

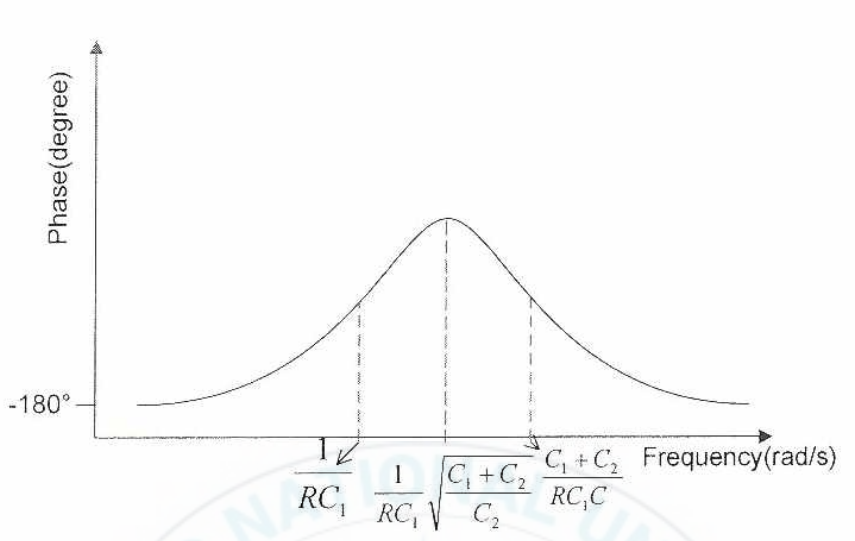


Figure 2.9 The phase characteristics of the third-order PLL.

Since the order of LPF with the magnitude of R, C_1 and C_2 affect the characteristics of the above equation, the stability and bandwidth should be thoroughly considered when designing the LPF.

Ⅲ. Designing a jitter characteristic improved PLL with RC time constant circuit

3.1 Structure of the proposed PLL

The proposed PLL is shown in Figure 3.1. It has the additional circuit such as the RC time constant comparator and the auxiliary CP to reduce the LPF voltage fluctuation. The RC time constant comparator is comprised of a voltage follower, an RC time constant circuit and a latch buffer. The RC time constant comparator controls the auxiliary CP according to the output voltage of the LPF. The auxiliary CP is connected to the LPF and additionally charge or discharge the LPF.

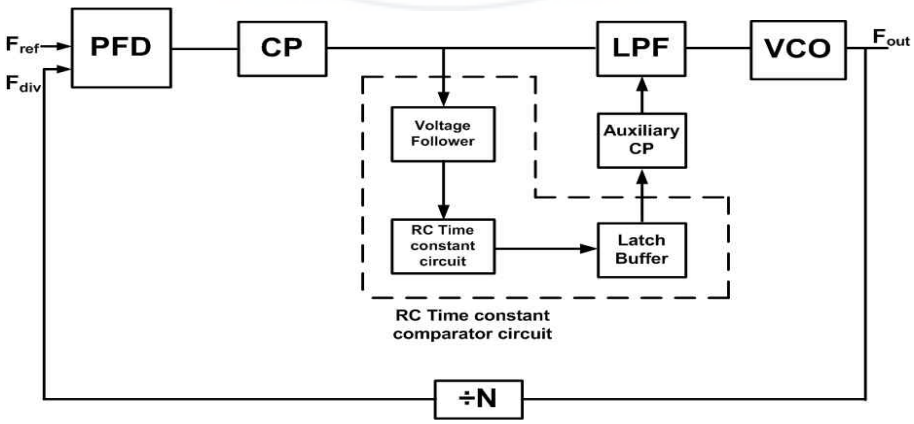


Figure 3.1 The proposed PLL

3.2 The operation principle of the RC time constant comparator circuit

Figure 3.2 is the RC time constant circuit. By utilizing the RC time constant, it makes two different signals and compares them to output the C_{OUT} that has a '0' or '1' value. C_{IN} is the transferred output voltage of the LPF through the voltage follower. V_{L1} is the first input signal of the comparator. Since it is transferred by the small RC time constant (R_{L1}*C_{L1}), the node V_{L1} shows a dynamic change like the output voltage of the LPF. V_{L2} is the second input signal of the comparator. Since it is transferred by the large RC time constant (R_{L2}*C_{L2} + R_{L3}*C_{L3}), the node V_{L2} operates like the constant signal that has the average value of the LPF output voltage. The difference of the RC time constant of the two input nodes, V_{L1} and V_{L2}, are compared and the comparator generates '0' or '1' output signals (C_{OUT}).

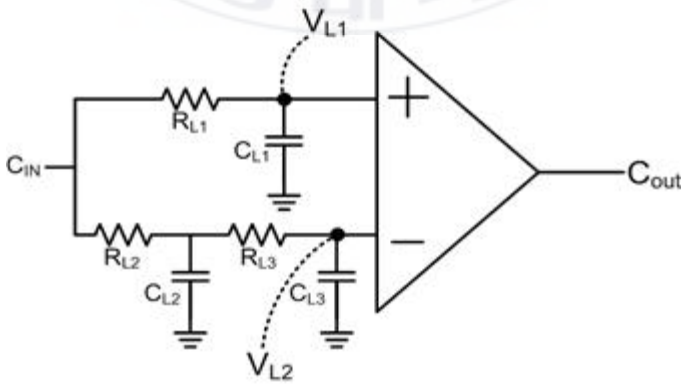


Figure 3.2 The RC time constant circuit.

Figure 3.3 shows the input and output signal of the comparator. The dynamically changing V_{L1} and the relatively static V_{L2} are shown in Figure 3.3. When V_{L1} is higher than V_{L2}, C_{OUT} outputs '1'. The '1' value of the C_{OUT} controls the auxiliary charge pump to discharge the LPF and decreases its voltage. On the other hand, when V_{L1} is lower than V_{L2}, C_{OUT} outputs '0' value. The '0' value of the C_{OUT} controls the auxiliary charge pump to charge the LPF and increases its voltage. As a result, the comparator detects the voltage fluctuation of the LPF and makes the total PLL circuit to have the minimum value of the voltage fluctuation.

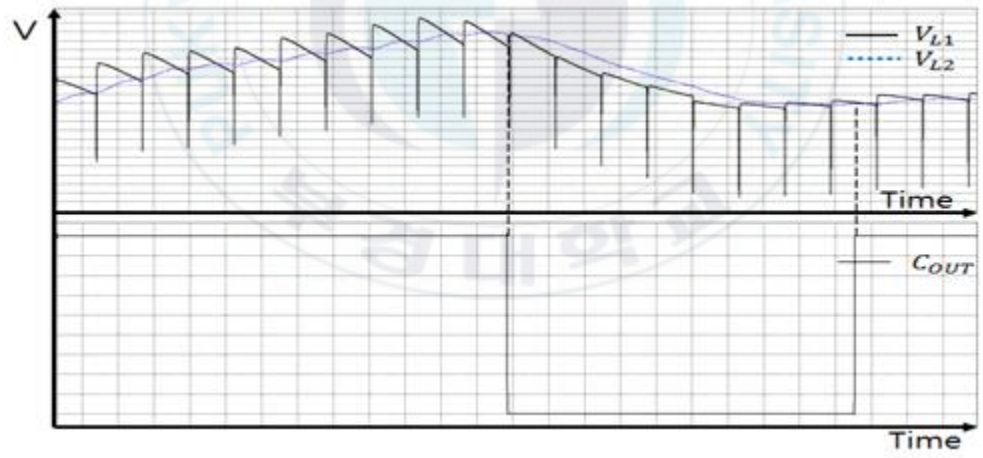


Figure 3.3 The input signals (V_{L1}, V_{L2}) and the output signal (C_{OUT}) of comparator.

When C_{OUT} has '1', the auxiliary CP operates like what is shown in Figure 3.4. Figure 3.5 shows V_{LPF} waveform of the conventional PLL and the proposed PLL as well. The LPF voltage on the PLL is increased during $\triangle t$ time that is generated by the UP pulse of the PFD during one period of reference signal. The charge flowing from Cp to Cz towards the end of the $T_{ref} - \triangle t$ decreases the excess phase shift per period and stabilizes the PLL. The proposed PLL is more efficient than the conventional PLL due to the fact that the RC time constant circuit additionally discharges the C_Z through the auxiliary CP and reduces the excess phase shift. Reduced voltage fluctuation of the LPF makes the output frequency of VCO steady and results in a considerable decrease in producing jitter.

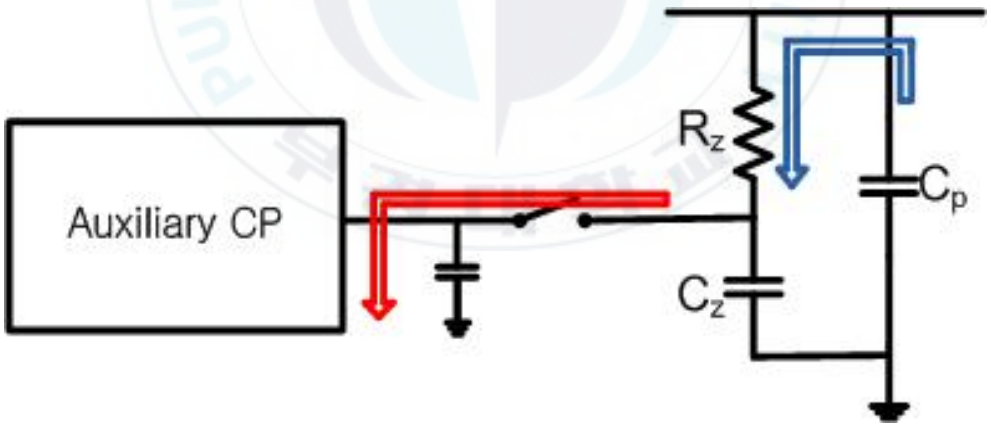


Figure 3.4 Operation principal of the auxiliary CP when C_{OUT} has '1' value.

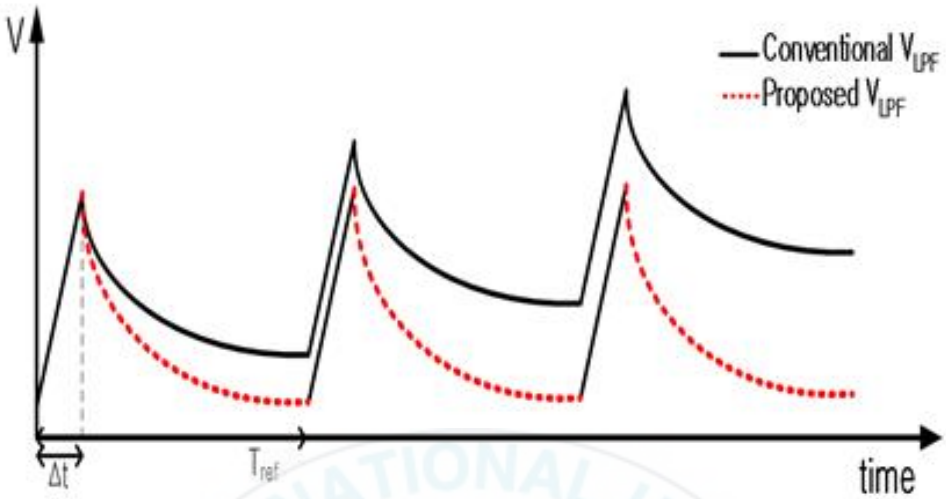


Figure 3.5 $\triangle\triangle V_{LPF}$ of conventional PLL and $\triangle\triangle V_{LPF}$ of proposed PLL when output voltage of loop filter increases.

3.3 Circuit design

3.3.1 Phase Frequency Detector (PFD)

In this paper, a simplified PFD with TSPC(True Single Phase Clock) CMOS logic circuit is installed in order to improve the speed of the PFD with the system that has been accelerated and integrated. The simplified TSPC CMOS logic circuit reduces the total chip area and power consumption, because the total number of MOSFET is decreased.

The proposed PFD is comprised of TSPC circuit as shown in Figure 3.3. The TSPC circuit is widely used because of its excellent performance in terms of simple structure, small power consumption and fast switching operation. D-F/F is composed of six MOSFET and the reset uses NOR circuit. Two phenomena can be observed on this PFD; First of all, when the difference between the reference signal and output signal of the VCO is very small, so-called dead zone problem occurs where the PFD is not able to detect the difference. Second, the UP and DN output signal of the PFD has impulse waveform close to the phase locked state. In order to solve the former problem and ensure enough switching time of CP according UP, DN signal, the delay cell is added at NOR gate output port.

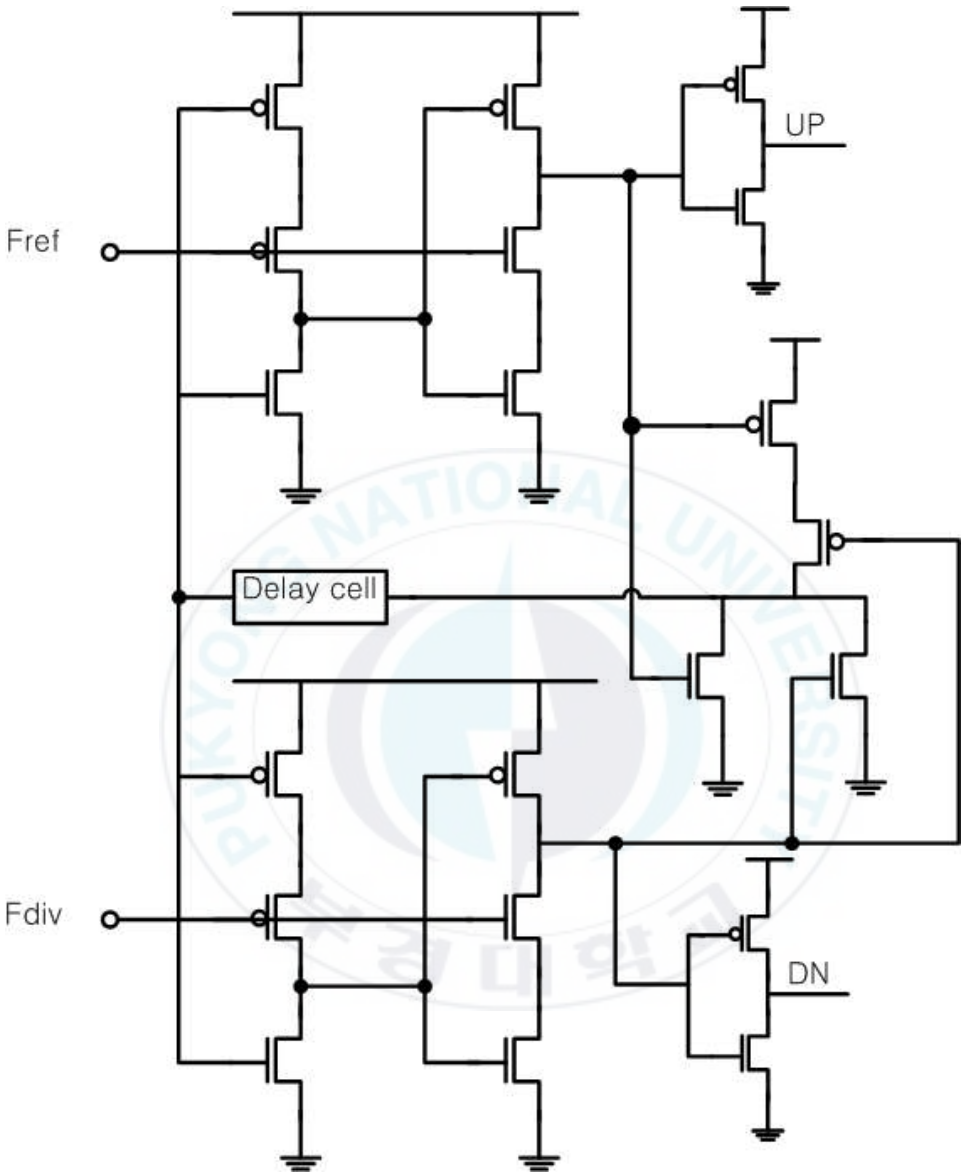


Figure 3.3 The circuit of the PFD.

3.3.2 Charge pump

After receiving UP and DN signals from the PFD, the CP transfers the current to the LPF voltage that is needed to control the VCO voltage. Since the CP directly affects the control voltage of the VCO, it should be carefully designed.

In the proposed structure, in order to eliminate the current mismatch that is arisen from the timing difference of the UP and DN signals after PLL is locked, UP/DN signal is connected with the input port of the CP through the latch buffer. Therefore, the UP/DN signal always occurs at the same time regardless of the change in the process. This latch buffer and the proposed CP are shown in Figure 3.4 and Figure 3.5. The clock-feedthrough and charge injection make redundant spur, which corresponds to the operation of the switches. The unit gain buffer that is connected with the output node of the CP suppresses that of the structural noise.

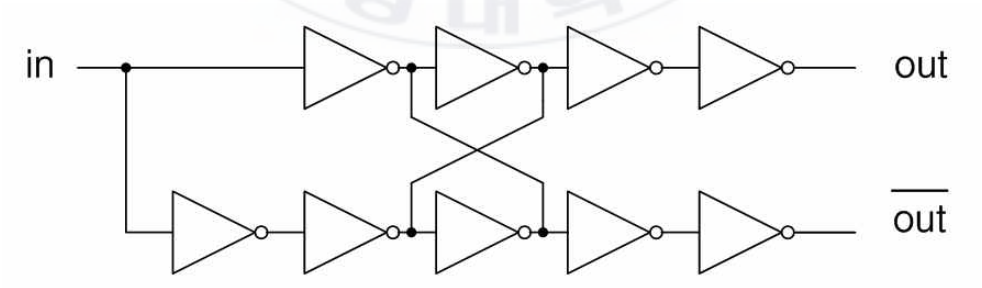


Figure 3.4 The latch buffer circuit.

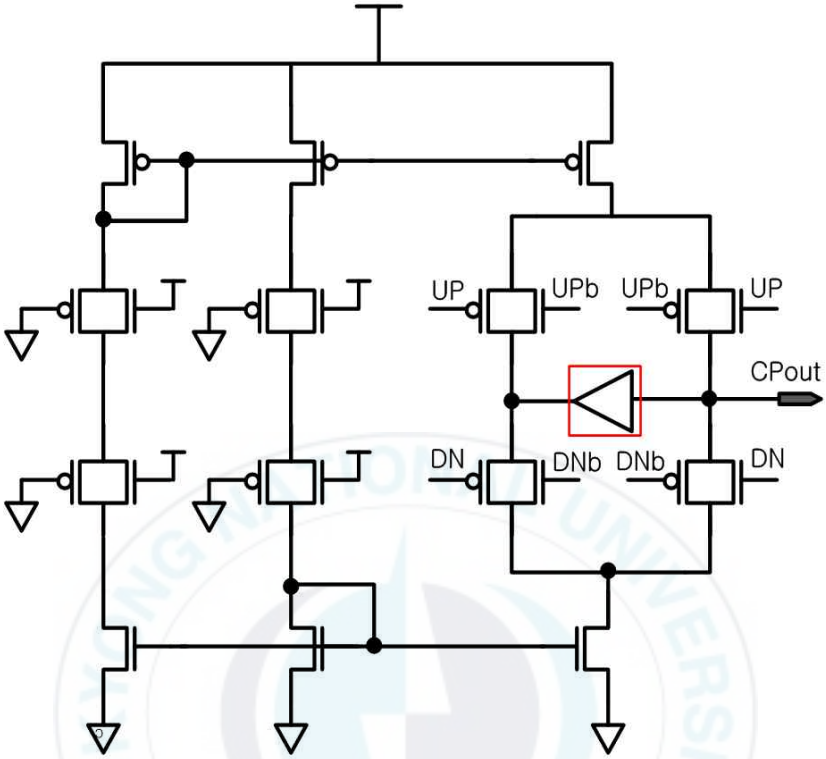


Figure 3.5 The proposed charge pump circuit.

3.3.3 Voltage controlled oscillator

VCR(Voltage Controlled Resistor) controls the delayed time of the VCO, which has a wide range of frequency bandwidth. The total block diagram, the differential delay cell of the VCO that includes VCR, and the input voltage versus frequency characteristics are shown in Figure 3.6 and Figure 3.7. The voltage of the LPF(V_{ctrl}) is transformed into the current that controls the delayed time of the VCO through VCR. The change in the input voltage of VCR is converted into a bigger change on the current, so the VCO is able to have a wider range of the frequency. VCO is comprised of the three differential delay cell. MP2&MP3 and MN2&MN3 reduce the phase noise by having a short on-time on the delay cell. MP1 and MP4, which are connected to the VCR, control the current that is flown into the delayed cell and the delayed time. The relation between the input voltage (V_{ctrl}) and the generated frequency can be shown in Figure 3.7. The Gain can be computed through the slope and it has K_{vco} = 330MHz/V. When the input voltage of the VCO is 1.2V, the output frequency is 1GHz as it is shown in the simulation.

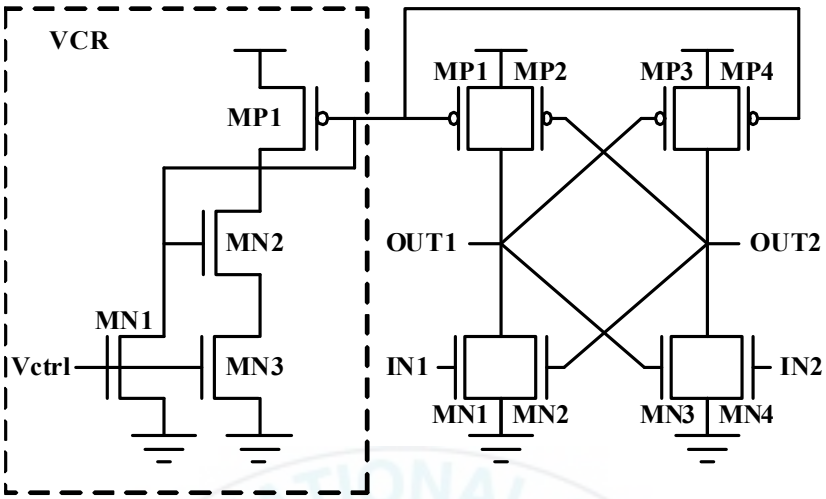


Figure 3.6 The differential delay cell of VCO and VCR.

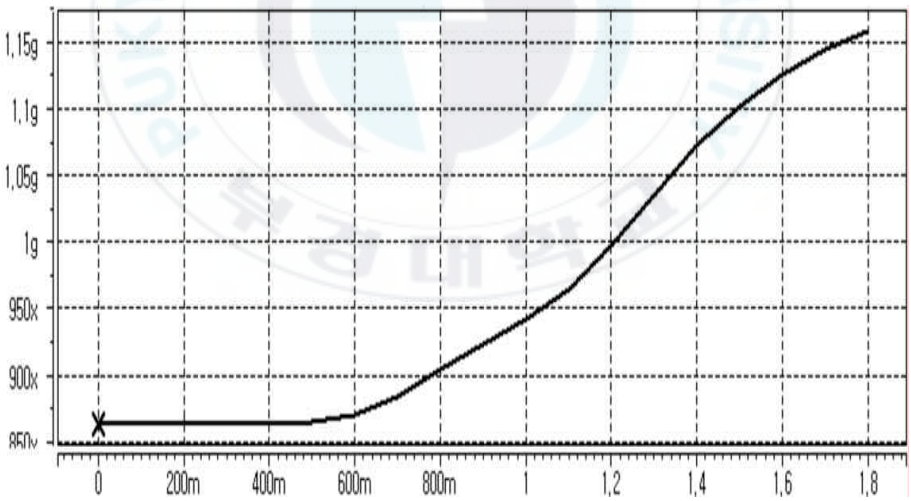


Figure 3.7 The V_{ctrl} - F_{out} characteristics.

3.3.4 Divider

The divider proposed in this paper is comprised of prescaler that can be divided-by-4 by using the dynamic E-TSPC (Expanded True Single Phase Clock) shown in Figure 3.8. On the back of them, the main divider has the digital control input port using the digital P&R which is able to make the division of 1 to 16. The 4 division prescaler drops the frequency of the VCO from high to low followed by the main divider which drops the even lower to 64 frequency division. The reason why the divider is made up of those structures is that the digital P&R layout block does not work well at high frequency. Using the prescaler that has no problem at high frequency makes the main divider to operate normally.

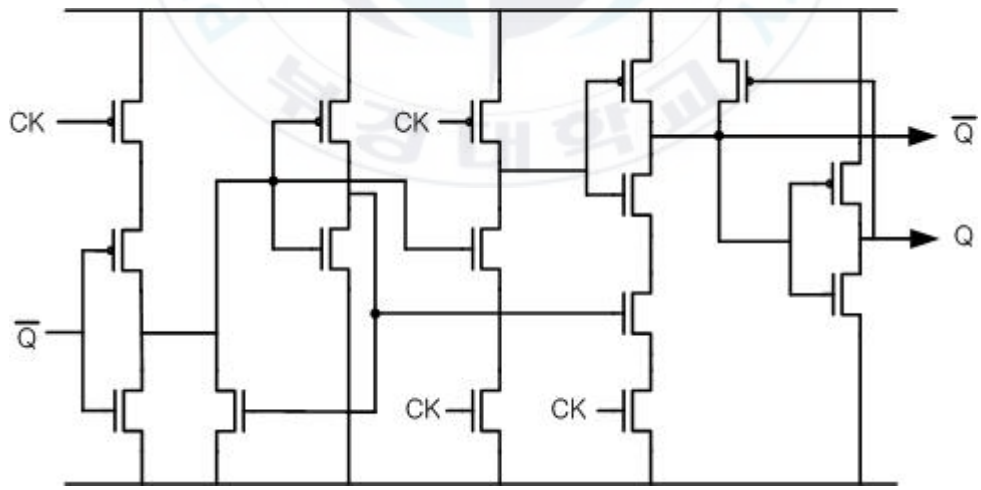


Figure 3.8 The dynamic E-TSPC (Expanded True Single Phase Clock)

3.3.5 Auxiliary charge pump

The schematic auxiliary charge pump is given in Figure 3.9. The output of the comparator (C_{OUT}) controls the switches on the auxiliary charge pump. These switches charge or discharge the capacitor C_X. When the C_{OUT} is at '1', the NMOS in the auxiliary charge pump discharges C_X to ground. When the C_{OUT} is at '0', however, the PMOS is used to charge C_X. SW_1 is controlled by the output signal of the VCO (F_{out}). SW_1 transfers the C_X charge to C_Z and consequently charges and discharges two capacitors on the LPF. As a result, the auxiliary charge pump controlled by C_{OUT} reduces the voltage fluctuation of the LPF.

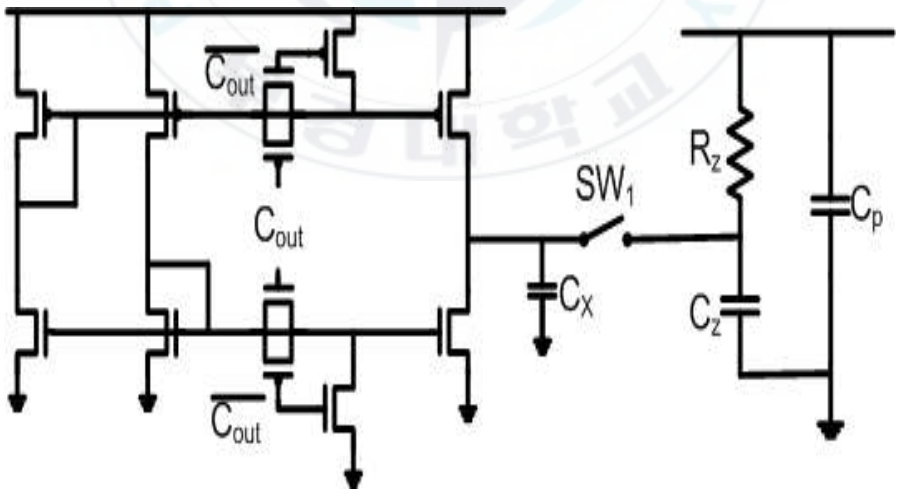


Figure 3.9 The auxiliary charge pump structure.

3.3.6 Voltage follower and comparator

The voltage follower is used to transfer the voltage of LPF to the comparator in order not to make an additional parasitic capacitance on the LPF. Its figure which is called the operational amplifier is shown in Figure 3.10.

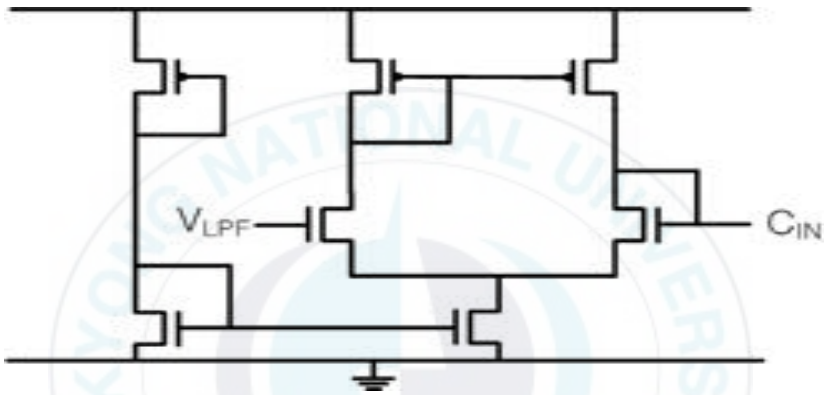


Figure 3.10 The voltage follower circuit.

The comparator circuit is shown in Figure 3.11. The comparator stably outputs 'high' or 'low' signals by using latch buffer

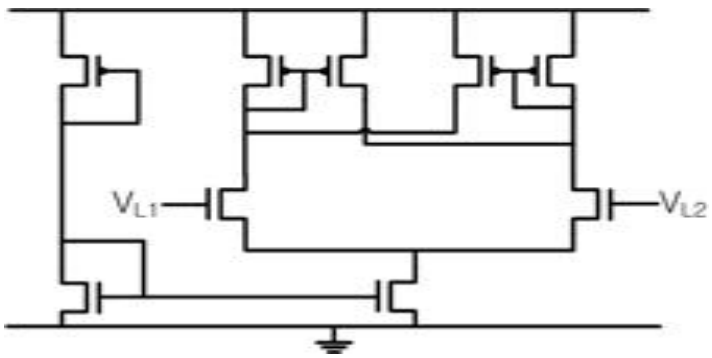
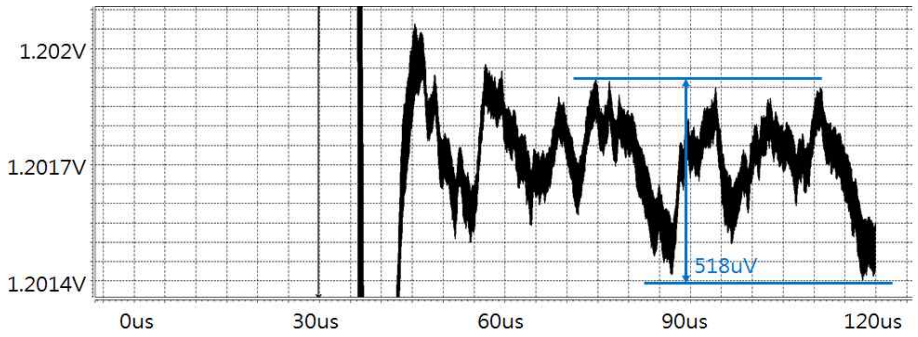


Figure 3.11 The comparator circuit.

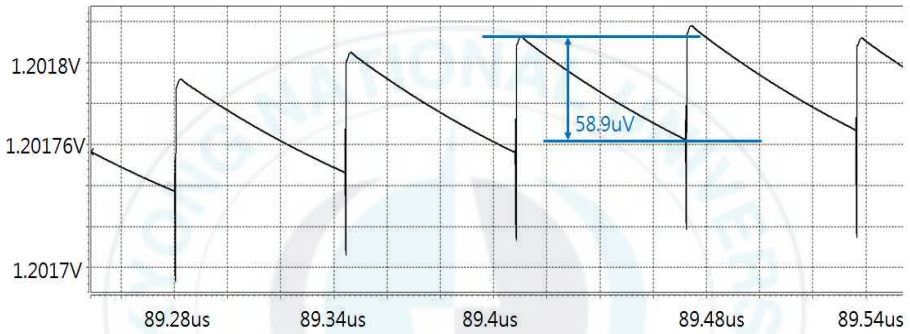
Ⅳ. Simulation result

4.1 Simulation result

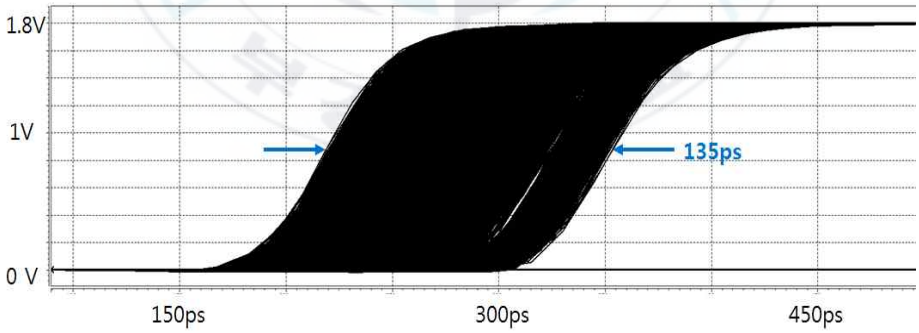
The proposed PLL is implemented in 0.18㎛ CMOS. It has 15.625MHz input frequency and outputs 1GHz frequency. The measurement of the conventional PLL is shown in Figure 4.1. The conventional PLL has △V_{LPF} = 518uV, △△V_{LPF} = 58.9uV and jitter = 135ps. However, the measurement of the proposed PLL is shown in Figure 4.2. The proposed PLL has △V_{LPF} = 334uV, △△V_{LPF} = 38.1uV and jitter = 65.8ps. The measurements of PLLs shows the performance of the newly designed PLL is better than that of the conventional PLL because of its smaller value of voltage fluctuation and jitter.



(a)

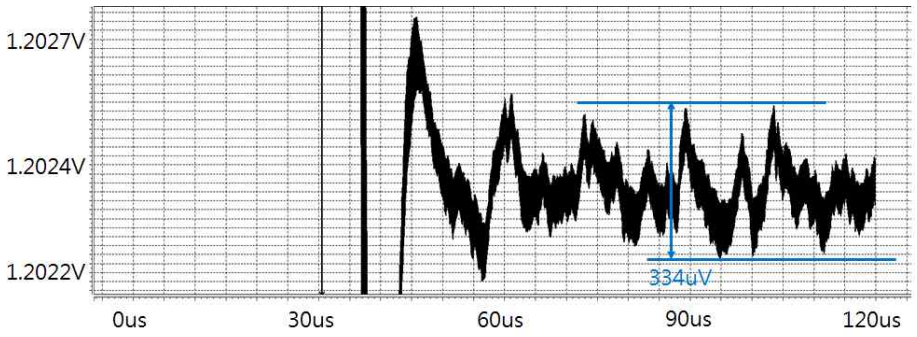


(b)

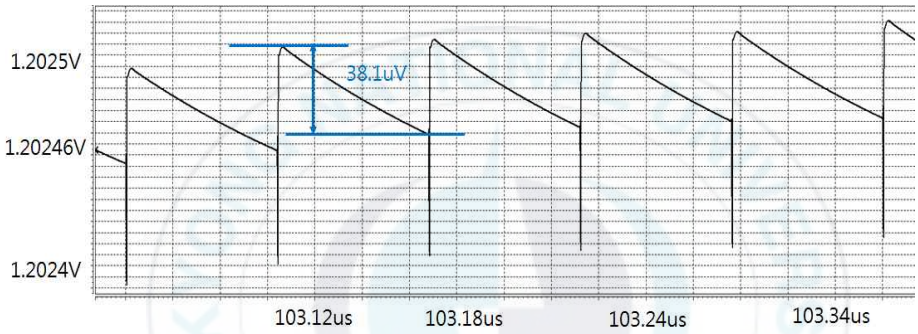


(c)

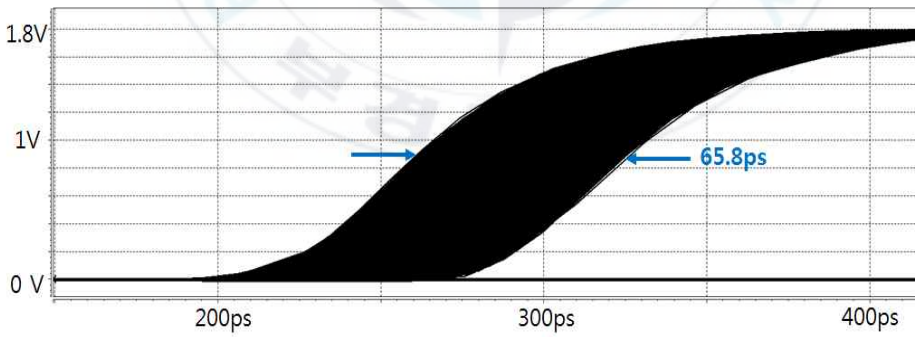
Figure 4.1 Simulation of the conventional PLL's (a)$\triangle V_{LPF}$, (b)$\triangle\triangle V_{LPF}$, and (c)jitter.



(a)



(b)



(c)

Figure 4.2 Simulation of the proposed PLL's (a)$\triangle V_{LPF}$, (b)$\triangle\triangle V_{LPF}$, and (c)jitter.

Ⅴ. Conclusion

In this paper, a new PLL with improved jitter characteristics with the RC time constant circuit is proposed. While one loop of the conventional PLL contributes stability of the total PLL circuit, the additional feedback loop of the proposed PLL performs better than the conventional PLL in terms of improving jitter performance by using the RC time constant comparator. Through the voltage follower, the voltage of the LPF is transferred to the RC time constant comparator with both small and large time constant value. The signal, which is passed through the small RC time constant, has the same value as the output voltage of the LPF. Another signal, which is passed through the large RC time constant, is transferred to comparator with long delay time and has signal that corresponds to the constant signal. The difference between the two signals outputs the control signal of the auxiliary CP. Depending on the output signal of the comparator the auxiliary CP additionally charges or discharges the voltage of the LPF. These operation of auxiliary CP limits the range of the voltage fluctuation of the LPF and results in stable output signal. On the proposed PLL, the application of the RC time constant comparator increases the chip size, but reduces the voltage fluctuation by 30% and jitter by 51.2%.

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