Dissertation for the Degree of Doctor of Philosophy

Low-Power High-Linearity CMOS Radio Frequency Receiver Frontend for 24GHz Automotive Collision Avoidance Radar

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24GHz 차량 충돌방지 저전력 고선형 CMOS 고주파 수신기 전단부

Advisor: Prof. Jee-Youl Ryu

by

Habibollah Rastegar

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Abstract

Communication has experienced explosive growth world-wide in the last decade and its huge market potential is driving relentless efforts in the information industry to improve the performance of wireless communication systems. Academia has also witnessed a flourish of research activities in communications, digital signal processing and radio frequency integrated circuit design.

Fuelled by the ever increasing demand for wireless products and the advent of deep submicron CMOS, RF ICs have become fairly commonplace in the semiconductor market. This has given rise to a new breed of Systems-On-Chip (SOCs) with RF front-ends tightly integrated along with digital, analog and mixed signal circuitry. However, the reliability of the integrated RF front-end continues to be a matter of significant concern and considerable

research. A major challenge to the reliability of RF ICs is the fact that their performance is also severely degraded by wide tolerances in on-chip passives and package parasitics, in addition to process related faults.

An RF front end receiver system refers to the analog down conversion stages of the wireless communication system. The Digital base-band signals cannot be transmitted directly through wireless channels due to the properties of electromagnetic waves. The baseband signals need to be converted to analog through a digital-to-analog converter (DAC), up converted to higher frequency using an up conversion mixer and then transmitted through the channel. The received signals are down converted to base band frequency and then converted to digital again using the analog to digital converter (ADC). The processes which the analog signal undergoes at the RF front end include amplification, mixing and filtering

The main wireless receiver task is to detect the desired modulated signals. Wireless receivers have to perform several functions such as tuning to the wanted signal carriers, filtering out the undesired signals, and amplifying the desired signal to compensate for power losses occurring during transmission. However, there are several receiver architectures, and the heterodyne and the direct conversion are the most popular.

In this dissertation, a modified IF receiver architecture is adopted as a compromise between the heterodyne and the direct conversion to have immunity against flicker noise, dc offset and I/Q mismatch, and to achieve higher integration. In a receiver frontend, either wired or wireless low noise amplifier (LNA) is the first gain stage after antenna. LNA should amplify all these signals without causing any significant distortion for the following

stage to handle. This sets the requirement of a certain gain to the LNA. Furthermore, the sensitivity of the receiver chain is determined by sensitivity of the LNA. This requires that a little noise from LNA must be introduced to the overall receiver.

Down conversion mixers as the next stage after LNAs in receiver frontend are more vulnerable than the other stages due to their configuration. They should translate the high frequency signals to either intermediate or baseband frequency ones.

Voltage-controlled oscillator (VCO) is an independent circuit, since some self-sustaining mechanism generates a periodic stable sinusoidal signal. VCO also can be used as a part of the frequency synthesizer to produce the local oscillator signal for both down/up-conversion mixers. An ideal VCO should meet most of these specification such as low phase noise, low power, wide tuning range, high integration, small die area accuracy and low cost.

This dissertation shows that significant benefits are achieved with continued design innovations in spite to the general belief that RF circuit design is a mature subject. With the down scaling of CMOS process, efforts in CMOS RFIC design has been continuing the future for long time.

1 Introduction

1.1 Motivation

Nowadays, road traffic crashes have become a major global concern. To enhance safety, automotive radar devices are now installing on many transport and luxury passenger vehicles. Automotive radars are utilized in advanced cruise control (ACC) systems which can provide information for driver, and actuate a motor vehicle's accelerator and/or brakes to control its distance separation behind another vehicle. Radar-based driver assistance systems also have other important functions such as collision warning systems, blind-spot monitoring, lane-change assistance, rear cross-traffic alerts and back-up parking assistance, collision mitigation systems and vulnerable road user detection.

Thanks to growing speed of radar-based collision avoidance systems, vehicles can see the other objects including pedestrian and other vehicles, anticipate accidents and collision, control the braking system and steering wheel to save the people life, and reduce the severity of collisions.

Radar transceivers are installed on the vehicles which operate in the all types of weather or sometimes both laser and camera are utilized to anticipate the imminent collision on the street or highways. At first, collision

avoidance systems search the surrounded area of the vehicles to detect the imminent crash. When the detection process is done, the system warns to the drivers by light, vibration in steering wheel or seat belt, and then the system based on the predefined distance fastens the seat belt and brakes, and finally controls the steering wheel to save the driver.

The main frequency bands of radar applications are 24GHz and 77GHz. For the sake of detection of other near vehicles in the medium-short range and wide beam, 24GHz is mainstream. The receiver for the automotive radar system operates in the band of 24 GHz frequency which is composed of low noise amplifier (*LNA*), downconversion mixer, and voltage-controlled oscillator (*VCO*).

1.2 Proposed Receiver Frontend Architecture

The main wireless receiver task is to detect the desired modulated signals. Wireless receivers have to perform several functions such as tuning to the wanted signal carriers, filtering out the undesired signals, and amplifying the desired signal to compensate for power losses occurring during transmission. However, there are several receiver architectures, and the heterodyne and the direct conversion are the most popular.

Typically, a heterodyne receiver translates the desired input RF signal onto one or more preselected intermediate frequencies before modulation. In this architecture, image rejection and IF filters are vital to avoid folding of interfering signals. Because of presence of several bulky and expensive RF/IF filters, the heterodyne architecture is not suitable for monolithic integration. Enforced by the trends to the cost and size of the RF frontend, alternative heterodyne architecture has been proposed. For instance, direct conversion technique converts the RF signals to the IF-zero baseband in the first frequency downconversion. Therefore, the receiver frontend can be realized in low cost and low power architecture due to the unnecessary off-chip IF filters. Despite superior performances of direct conversion architecture, it suffers from the dc offset and LO leakage which leads to complicate the design and implement of individual blocks to relax the specifications of system.

A modified IF receiver architecture is adopted as a compromise between the heterodyne and the direct conversion to have immunity against flicker noise, dc offset and I/Q mismatch, and to achieve higher integration. The block diagram of the proposed receiver frontend is illustrated in Figure 1.1. First, LNA amplifies the incoming RF signal at 24 GHz. Then the amplified

signal is down-converted to a low IF of 10 MHz by the first and second mixer stages. It is noted that the quadrature LO signals required for the second mixer are generated by dividing the first LO signal by 2.

The unwanted image signal can be attenuated approximately 20 dB by exploiting narrow band characteristic which is provided in the input port of LNA. A LO frequency of 16 GHz is applied to the first mixer to generate signals at an IF band of 8 GHz. Furthermore, the finite bandwidth of receiver frontend leads suppressing of the spurious band of 40 GHz which is generated by the first mixer stage. A divided-by-2 extended true-single-phase-clock (*E-TSPC*) frequency divider is also designed to provide the quadrature LO signals required for the second mixer stage. Therefore, the output signals of the second mixer stage are located at 10 MHz. In order not to use off-chip components such as buffer, balun and filters, an active balun is adopted to perform three tasks as follows: (*i*) convert the differential output of the second mixer to single-ended output for simulation of the frontend performances; (*ii*) match the output ports of the whole circuits to *50*Ω to achieve S_{22} of less than -10 dB; (*iii*) filter out the undesired image and spurious signals.

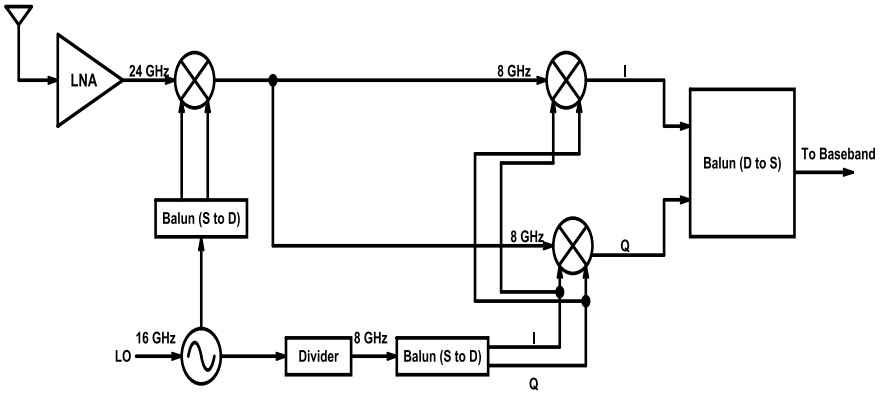


Figure 1.1: Proposed 24 GHz receiver frontend

1.3 Objectives

The overall 24 GHz receiver frontend blocks including LNA, downconversion mixer, and VCO are presented in this dissertation. The proposed frontend aims to the radar-based collision avoidance applications. The objective of this dissertation is as follows:

- New receiver frontend architecture has been invented to fulfill the radar-based collision avoidance application criteria. Direct conversion receiver (*DCR*) is the best candidate among the various receiver architectures due to the low cost and low power issues. However, large dc offset, local oscillation (*LO*) leakage, flicker (*1/f*) noise, and I/Q mismatch are the

bottlenecks of DCR receiver. To alleviate these problems, single intermediate frequency (*IF*) DCR architecture has been proposed with the advantage of both the super-heterodyne and DCR architectures. In this receiver type, at first, the incoming signal is converted to IF and then again it is converted to baseband frequency. This operation alleviates the specifications of the receiver backend and enables the analog-to-digital conversion at low frequencies

- To prove the validity of each block in the receiver frontend, a set of new mathematical formulas is given.
- New LNA has been designed, implemented, laid out and finally fabricated. The promising measurement results show that this LNA is potent for *RF* applications such as the radar-based collision avoidance. The designed LNA has unique structure and its features have been proved by mathematical equations The measurement results show the feasibility of the proposed circuit for wireless portable devices.
- The second block in receiver frontend is downconversion mixer. In the new implemented circuit, the LNA and mixer are combined to reduce the power consumption and increase the linearity of the overall receiver. The mixer circuit is employed in IF direct conversion receiver (*IF-DCR*) to

reach the predefined characteristics such as low noise, and low power consumption.

- New VCO is designed, implemented and laid out to generate the sine wave signal for the switching stage. To the best of author′s knowledge, the proposed VCO has the lowest power consumption in comparison with the other similar works. High output swing and low phase noise as well are the great achievement from the new idea.
- Low power Baluns are designed to convert the differential input/output to single input/output or vice versa. The buffers are implemented by measuring purpose.

1.4 Overview

The dissertation is organized as follows. In Chapter 2, the first block of receiver frontend known as LNA is presented. First, the background of LNA is presented and then the fundamental features of LNA are defined. These basic characteristics help the readers to get familiar with LNA parameters and the existing trade-offs between the output results of LNA which provide at the end of this chapter. After fundamental section, the new idea of LNA is proposed and proved with mathematical equations in depth detail. The

measurement results verify the validity of the new designed circuit for RF applications. The layout and die microphotograph of the proposed LNA are also presented. The comparison of the proposed idea with recently published works is given as well.

The overview of downconversion mixer is described and explained at the beginning of Chapter 3. Then different types of active mixer configurations are presented with pointing out to their advantages and disadvantages. At the end of Chapter 3, the new mixer topology is designed to reach the predefined characteristics such as low power consumption, high conversion gain (*CG*), and low noise figure (*NF*). The summary of this work is presented along with a table to bold the advantages of the new architecture.

Chapter 4 reviews the general features of the VCO. The background and fundamental issues of VCO are expressed in the first sections. On the continue, the major parameters of LC VCO are presented and the tradeoffs among them are given. The proposed circuit for RF application is presented. The implemented circuit is aimed for low power consumption, low phase noise and high output swing. To measure the result, two buffers are placed at the end of LC VCO.

In Chapter 5, the overall receiver frontend circuit is presented. The different blocks of receiver chain are integrated and placed on a single chip. Each block including LNA, mixer, and VCO is analyzed and explained in depth detail. The unique frontend architecture achieves high gain, low power consumption, and high linearity for the radar-based collision avoidance applications. The results of the proposed frontend with high level of integrity are illustrated at the end of this chapter. The layout of the receiver frontend is drawn as well.

By integrating the two-stage LNA and downconversion mixers, the frontend has been designed in 130-nm CMOS technology. The LNA stage was adopted on complementary push-pull (*CPP*) topology to boost the gain and the linearity of whole circuit. Meanwhile, the LNA was realized in folded configuration to reduce power supply and to increase voltage headroom. The frontend was realized in IF-DCR architecture to increase integration level and alleviate the DCR problems. Two active baluns were also designed to increase the integrity of the frontend. Furthermore, the switch transistors were biased in subthreshold region to reduce the power consumption.

Chapter 6 concludes this dissertation and the further future investigation of this area is suggested at the end of this chapter.

2 Design of Low Noise Amplifier

2.1 Background

In a receiver frontend, either wired or wireless low noise amplifier (*LNA*) is the first gain stage after antenna. At the same time, it must meet several specifications which make its design really challenging. Signal coming from the receiver antenna at the input of LNA is very small and usually varies from less than *-130dBm* to *-70dBm*. Therefore, LNA should amplify all these signals without causing any significant distortion for the following stage to handle. This sets the requirement of a certain gain to the LNA. Furthermore, the sensitivity of the receiver chain is determined by sensitivity of the LNA. This requires that a little noise from LNA must be introduced to the overall receiver. According to Friis equation, gain of LNA should be as high as possible to suppress the noise of subsequent blocks. In other words, a certain signal-to-noise ratio (SNR) is required for the LNA to detect the coming signal reliably, and hence noise added by the circuit should be reduced as much as possible, which will set the noise requirement of the LNA.

Low-pass filter (LPF), high-pass (HPF) and band-pass filter (BPF) are located before and after LNA to delete and reduce the unwanted signals.

The transfer function of the filter is usually a dependent variable of termination impedance. Based on IEEE standards, there are specific input/output termination impedances, i.e. *50*Ω or *75*Ω on the LNA. The LNA noise is also a function of source impedance. It's noteworthy that the optimum source impedance for minimum noise figure might be different from the one required for the preceding stage, e.g. 50Ω. There are trade-offs between gain, noise figure and input/output matching impedance.

The receiver chain has to be able to minimize or cancel the adverse effects of large number in-band interferences and inter-modulation/cross-modulation caused by transmitter leakage or blockers. Thus, to have a reasonable signal reception the circuits should be sufficiently linear. Low power consumption is another constraint for mobile and portable applications.

LNA design involves trade-offs among many figures of merits such as gain, noise, power dissipation, input matching, stability, and linearity [1]. Such an amplifier must feature wideband input matching to a 50Ω antenna, flat gain over the entire bandwidth, good linearity, minimum possible noise figure, and low power consumption [2].

A careful study is required to satisfy all the above-mention trade-offs in designing either narrowband or wideband LNA. To achieve this goal one

needs to provide an analytical model for the LNA and find the equations for the LNA characteristics such as gain, linearity and noise figure.

2.2 S-parameters

Scattering parameters, which are commonly referred as S-parameters are widely used in design and analysis of microwave and RF circuits. A parameter set is used in S-parameters that relates to the traveling waves that are scattered or reflected when an n-port network is inserted into a transmission line.

To characterize an n-port linear network, S-parameter analysis is basically used as a modelling method. H-parameters, Y-parameters and Z-parameters are other methods to characterize the n-port network. Since they are behavioural modelling methods, we can put all of them into the same category for a network. The device or n-port network is assumed as a black box, and only the interaction between the ports and outer environment is modelled. For instance, in low frequencies, H-, Y-, or Z-parameters are widely used since voltage and current are the variables to find the transfer function. However if we want to use H-, Y-, or Z-parameters, some problems arise for relatively high frequencies.

For applying short and/or open circuit condition at each port in H, Y or Z measurement, it is hard especially to RF bands. Active devices such as transistors and tunnel diode very often cannot be connected in stable short or open circuit conditions.

S-parameters, on the other hand, are usually measured with the device embedded between a 50Ω load and source, and there is very little chance for oscillations to occur. Another important advantage of S-parameters stems from the fact that traveling waves unlike terminal voltages and currents do not vary in magnitude at points along a lossless transmission line. This means that S-parameters can be measured on a device located at some distance from the measurement transducers.

The behaviour of the two-port network in Figure 2.1 can be described by the linear equations using S-parameters as defined in Eqs. (2.1) and (2.2).

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.2}$$

where a_1, a_2,b_1 and b_2 are traveling wave.

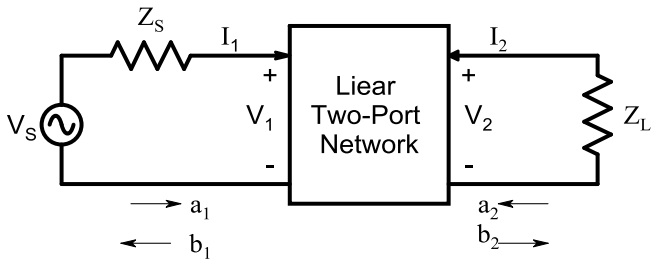


Figure 2.1: Two-port network for incident waves (a_1, a_2) and reflected waves (b_1, b_2) used in S-parameters definitions

The S-parameters are defined as defined in Eqs. (2.3) to (2.6).

$$S_{11} = \frac{b_1}{a_1}|_{a_2=0} \tag{2.3}$$

$$S_{22} = \frac{b_2}{2}|_{a_1=0} \tag{2.4}$$

$$S_{21} = \frac{b_2}{a_1}|_{a_2=0} \tag{2.5}$$

$$S_{12} = \frac{b_1}{a_2}|_{a_1=0} \tag{2.6}$$

For simplicity in measurement and calculation, we assume that both input and output ports are real and positive, and have same reference impedance of Z_0.

The independent variables a_1, a_2, b_1 and b_2 can be related to port voltages (V_1, V_2) and currents (I_1, I_2) as expressed in Eqs.v(2.7) to (2.10).

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{i1}}{\sqrt{Z_0}} \quad (2.7)$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{i2}}{\sqrt{Z_0}} \quad (2.8)$$

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{r1}}{\sqrt{Z_0}} \quad (2.9)$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{r2}}{\sqrt{Z_0}} \quad (2.10)$$

where $V_{i1} = \frac{V_1 + I_1 Z_0}{2}$ and $V_{i2} = \frac{V_2 + I_1 Z_0}{2}$ are incident voltage waves on port 1 and 2 respectively.

$V_{r1} = \frac{V_1 - I_1 Z_0}{2}$and $V_{r2} = \frac{V_2 - I_2 Z_0}{2}$ are reflected voltage waves from port 1 and poert 2 respectively.

$|a_1|^2$ is the incident power on the input of the network, and it is also the available power from source impedance Z_0. $|b_1|^2$ is the reflected power from the input port of the network, or the available power from a Z_0 source minus the power delivered to the input of the network. $|a_2|^2$ is the incident power on the output of the network, and it is also the reflected power from the load. $|b_2|^2$ is the reflected power from the output port of the network, or the incident power on the load which is also the power delivered to a Z_0 load.

The expressed S-parameters related to the mentioned definition of a_1, a_2, b_1 and b_2 are as follows:

$$|S_{11}|^2 = \frac{Refelected\ power\ from\ input\ network}{Incident\ power\ on\ the\ input\ network} \quad (2.11)$$

$$|S_{22}|^2 = \frac{Refelected\ power\ from\ output\ network}{Incident\ power\ on\ the\ output\ network} \quad (2.12)$$

$$|S_{21}|^2 = \frac{Power\ deliverd\ to\ Z_0\ load}{available\ power\ from\ Z_0\ source}$$

$$= Transducer\ power\ gain\ with\ Z_0 load\ and\ source \quad (2.13)$$

$$|S_{22}|^2 = Reverse\ trabsducer\ power\ gain\ with\ z_0 \text{ load and source} \quad (2.14)$$

2.3 Power Gain

The input/output impedance matching network and RF transistor are the parameters which determine and control the gain performance for a RF amplifier such as LNA. Consider the basic block diagram of an amplifier shown in Figure 2.2. The amplifier is modeled by its S-parameters and terminated by arbitrary source and load impedance, Z_S and Z_L. S_{11} and S_{22} are the input and output reflection coefficients with Z_0 source and load terminations, respectively.

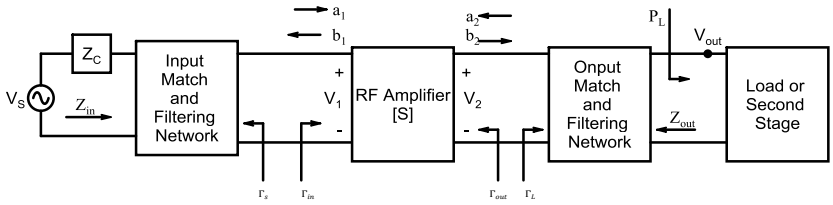


Figure 2.2: Block diagram of single-stage RF amplifier

The input and output reflection coefficients Γ_{in} and Γ_{out} for a network with an arbitrary impedance termination can be described as Eqs. (2.15) and (2.16) [3].

$$\Gamma_{in} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{2.15}$$

$$\Gamma_{out} = \frac{b_2}{a_2} = S_{22} + \frac{S_{11}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \tag{2.16}$$

where $\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}$ and $\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$ are the source and load reflection coefficients, respectively.

The amplifier reaches its maximum power transfer function if at the same time the input and output are complex conjugate matched, i.e. $\Gamma_{in} = \Gamma_S^*$ and $\Gamma_{out} = \Gamma_L^*$. When S_{12} is approximately or practically zero, the amplifier is so called bilateral ($S_{12}=0$). In bilateral case, $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$ which means impedance matching at the input and output ports can be done separately and these ports are decoupled from the other one.

There are several gain definitions for an amplifier. Power gain (G) is defined as the power delivered to the load divided by the power inserted to the network. Available power gain *(GA)* shows the maximum possible power amplification of the amplifier.

The voltage gain (A_v) is defined as the voltage at the output port divided by the voltage at the input port of the amplifier as expressed in Eq. (2.18) [3].

$$A_v = \frac{V_2}{V_1} = \frac{S_{21}(1+\Gamma_L)}{(1-S_{22}\Gamma_L)(1+\Gamma_{in})} \tag{2.17}$$

The transducer power (G_T) is defined as the power delivered to the load divided by the power available from the source [3]

$$G_T = \frac{P_L}{P_{AVS}} \tag{2.18}$$

where P_L is defined as:

$$P_L = |b_2|^2(1 - |\Gamma_L|^2). \tag{2.19}$$

P_{AVS} is also defined as

$$P_{AVS} = \frac{|b_2|^2}{1-|\Gamma_S|^2}. \tag{2.20}$$

where $b_s = \frac{V_s\sqrt{Z_0}}{Z_s+Z_0}$.

Thus,

$$G_T = \left|\frac{b_2}{b_s}\right|^2 (|1-\Gamma_s|^2)(|1-\Gamma_L|^2) \quad (2.21)$$

Using the signal flow chart, the ratio $\frac{b_2}{b_s}$ can be given as

$$\frac{b_2}{b_s} = \frac{S_{21}}{(1-S_{11}\Gamma_s)(1-S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_s\Gamma_L} \quad (2.22)$$

Finally, the transducer power gain is expressed as

$$G_T = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{(1+S_{11}\Gamma_s)(1+S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_S\Gamma_L} \quad (2.23)$$

For a bilateral, i.e. S_{12} is very small and effectively zero, Eq. (2.23) can be approximated as Eq. (2.24).

$$G_T = \frac{1-|\Gamma_S|^2}{|1+S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1+S_{22}\Gamma_L|^2} = G_s|S_{21}|^2G_L \quad (2.24)$$

This current formula is in terms of reflection coefficients and input/output return losses. We offer to re-write the above equation in terms of impedances to explicitly reflect the effect of IMF. It can be obtained maximum power

gain when both the input and output ports are complex conjugate matched (i.e., $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$). The maximum power gain (G_{max}) is given as:

$$G_{max} = \frac{1}{1-|S_{11}|^2}|S_{21}|^2\frac{1}{1-|S_{22}|^2} \tag{2.25}$$

Now available power gain of the LNA can be written as the multiplication of the maximum power gain and IMF, if there is an impedance mismatch at the input port of the LNA.

$$G_{LNA} = \underbrace{\frac{4R_S R_{in}}{(Z_{in}+Z_S)^2}}_{IMF} G_{max} \tag{2.26}$$

where Z_{in} are Z_S are the input and source impedances shown in Figure 2.2.

2.4 Stability Factor

Stability is also a very important parameter of RF amplifier. The other parameters such as gain, noise figure are meaningful when the amplifier is stable. By assuming the input impedance at the input port of the amplifier $Z_i = R_i + jX_i$, then the Γ_{in} is expressed in Eq. (2.27):

$$\Gamma_{in} = \left|\frac{Z_i - Z_0}{Z_i + Z_0}\right| = \sqrt{\frac{(R_i - Z_o)^2 + X_i^2}{(R_i + Z_o)^2 + X_i^2}} \tag{2.27}$$

If the real part of the input resistance R_i is negative, i.e. $R_i < 0$, then $|\Gamma_{in}| > 1$. Oscillation can occur if the loss coms from the input termination network compensated by negative resistance. The amplifier is potentially unstable. We have same scenario for the stability issue of output port. Therefore, the amplifier is unconditionally stable if for all the passive terminations at the input and output ports, Eqs (2.28a) and (2.28b) would be satisfied. Otherwise, it is potentially unstable or conditionally stable.

$$|\Gamma_{in}| < 1 \tag{2.28a}$$

$$|\Gamma_{out}| < 1 \tag{2.28b}$$

In term of S-parameters, it can be expressed that the amplifier are unconditionally stable if it has the following conditions.

$$|S_{11}| < 1 \tag{2.29a}$$

$$|S_{22}| < 1 \tag{2.29b}$$

$$K > 1 \tag{2.29c}$$

where k is the stability factor given by Eq. (2.30).

$$K = \frac{1-|S11|^2+|S22|^2+|S11*S22-S12*S21|^2}{2|S12*S21|} > 1 \quad (2.30)$$

Adding a shunt conductance or a series resistance to the unstable port is the simple method to stabilize an active device. Practically, since the input and output ports of the amplifier are coupled to the other, it is usually enough to stabilize one of the ports. One should not add a series resistance or a shunt conductance to the input port of the amplifier, since it will cause additional noise to be amplified. Therefore, the best way is to stabilize the output port.

2.5 Noise

In communication systems, undesired signal is called noise, and noise reduces the sensitivity of the overall system. There are a variety of noise sources with different noise generation. In the integrated circuits the dominant sources of noise are shot noise, flicker noise, and thermal noise. Shot noise is mainly caused by the hopping of electric charges over a potential barrier, and it is specific to nonlinear devices such as diodes and transistors. In MOS devices, the only source of shot noise is the dc gate leakage current, and hence it is not considered a major problem [4]. In Bipolar Junction Transistor (BJT) base and collector shot noise are the main

sources, and they may significantly degrade the performance of the overall receiver.

Flicker noise, also known as pink noise, occurs due to the trapping of charges in the defects and impurities of the channel region in MOS devices [4]. As can be seen from the Eq. (2.31), flicker noise is inversely proportional to the operational frequency (f). In the other words, larger MOS devices with large *W* lead to less flicker noise. The spectral density of this noise is given by Eq. (2.31).

$$\overline{\iota_{fn}^2} = \frac{K.g_m^2}{fWLC_{ox}{}^2} \tag{2.31}$$

where *K* is a device geometric constant, *W* and *L* are the width and length of the MOS device, , C_{ox} is the gate-oxide capacitance per unit area, and g_m is the trans-conductance of the MOS device, respectively.

Therefore, at very low frequencies the dominant noise source is flicker noise. Flicker noise does not play an important role LNAs because the frequency range of the received signal is several gigahertzes, and hence it can be ignored. It is noteworthy that in mixers or voltage controlled

oscillators (*VCOs*) flicker should be considered and it can be a major problem.

2.5.1 Noise Sources

The generic small signal model of a cascode topology with noise sources is shown in Figure 2.3. There are four sources of noise. It contains the thermal noise of source resistance ($i_{n,\mathrm{Rs}}$), thermal noise of the channel current ($i_{n,d}$), the gate-induced current noise ($i_{n,\mathrm{g}}$), and the thermal noise of the output resistance ($i_{n,out}$). The power spectral densities (*PSDs*) of $\overline{i_{n,Rs}^2}$ and $\overline{i_{n,Rout}^2}$ are as Eqs. (2.32) and (2.33).

$$\overline{i_{n,Rs}^2} = 4kT\frac{1}{R_s}\Delta f \tag{2.32}$$

$$\overline{i_{n,Rout}^2} = 4kT\frac{1}{R_{out}}\Delta f \tag{3.33}$$

where T is the absolute temperature in Kelvin, Δf is the noise bandwidth in Hz and k is the Boltzmann constant.

The PSDs of channel current thermal and gate-induced noises are given by Eqs. (2.34) and (2.35)[5-6].

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f \tag{2.34}$$

$$\overline{i_{n,g}^2} = 4kT\delta g_g\Delta f \tag{2.35}$$

where g_g is the equivalent shunt gate conductance, given by Eqs. (2.36) [5].

$$g_g = \frac{(\omega C_{gs})^2}{5g_{d0}} \tag{2.36}$$

where g_{d0} is the drain conductance for zero drain-source voltage and γ is a technology-dependent parameter with a value of approximately 2/3 for long-channel devices in saturation region (in short channel devices γ is larger and its value is between 2 and 3) [7]. δ is the gate noise coefficient and is also a technology-dependent parameter. The value of δ is 4/3 for long channel devices and it is augmented by a factor of 2 in short channel devices.

2.5.2 Noise Figure

Noise figure (*NF*) is measurement factor of degradation of signal-to-noise ratio (*SNR*) as the incoming signal from antenna traverses the receiver frontend. Mathematically, noise figure is defined as the ratio of the input SNR to the output SNR of the system as expressed in Eq. (2.37).

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{output\ noise\ power\ due\ to\ source}{total\ output\ noise\ power} \quad (2.37)$$

NF can be defined in two ways, for each block separately or the entire receiver. The LNA noise NF_{LNA} determines the inherent LNA noise, added to the desired or wanted signal during the process of amplification.

According to the classical two-port network, NF of a noisy two-port network can be written as Eq. (2.38).

$$NF = NF_{min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \quad (2.38)$$

where NF_{min} is the minimum achievable NF, B_{opt} and G_{opt} are the optimum source susceptance and conductance corresponding to NF_{min}, and R_n is an equivalent noise resistance, which quantifies the sensitivity of NF to departure from optimum conditions and B_S and G_s are the source susceptance and conductance.

NF is a function of source admittance looking into the input terminal of the two-port network. To achieve the NF_{min}, an optimum admittance, namely Y_{opt}, should be introduced to the network. The expressions for NF_{min} and Y_{opt} can be derived for a MOS device by considering a two-port network model for the MOS device. In this model the gate-source terminal is the input port, and the drain-source terminal is the output port.

The small signal model of a MOS device which consists of all noise sources connected to the noise source $\overline{i_s^2}$ and the source admittance $Y_s=G_s+jB_s$ are shown in Figure 2.3.

We assume that in MOS devices $\overline{i_{n,\mathrm{g}}^2}$ and $\overline{i_{n,\mathrm{d}}^2}$ are dominant noise sources and for the noise parameters and NF_{min} can be obtained in Eqs. (2.39) to (2.42).

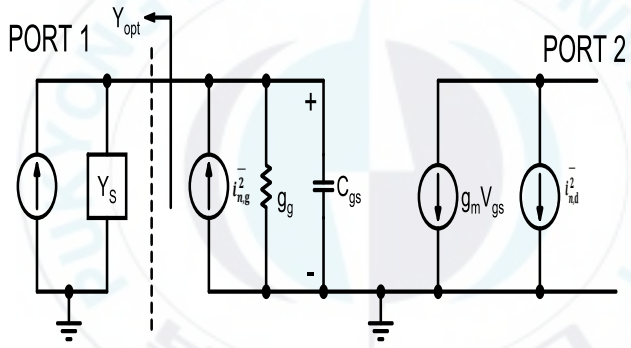


Figure 2.3: MOS model of two-port network for noise calculations

$$R_n = \frac{\gamma g_{d0}}{g_m^2} \tag{2.39}$$

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{2.40}$$

$$G_{opt} = -\omega C_{gs}(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \tag{2.41}$$

$$NF_{min} \approx 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_t}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \quad (2.42)$$

where $\alpha = g_m/g_{d0}$ equal to one for long channel devices and, it decreases as devices shrink to smaller dimensions.

It is obvious from Eq. (2.42) that with the increasing transition frequency (f_t) the minimum noise figure decreases. It should be noted that as CMOS scaling down, the transion frequency increases. Therefore, employing CMOS technology will be an advantage for having low noise figure.

2.5.3 Output Noise of the First Stage

The input impedance of the cascode topology using inductively degenerated technique will explain in Section 2.7. Figure 2.4 shows small-signal model of a cascade topology with inductively degenerated noise sources. The input impedance should be equal to the source impedance R_s, and it can be expressed as Eq. (2.43).

$$Z_{in} = g_m \frac{L_s}{C_t} = R_s = 50\Omega \quad (2.43)$$

where L_s is the source inductor, C_t is the total capacitance seen from source.

The quality factor of input circuit is then

$$Q = \frac{1}{(R_s + g_m \frac{L_s}{C_t})\omega_0 C_t} = \frac{1}{2R_s \omega_0 C_t} \tag{2.44}$$

where ω_0 is the resonance frequency of input matching network.

The output noise ($i_{n,out}$) of four noise sources (shown in Figure 2.4) at ω_0 is as described in Eq. (2.45) to (2.48).

$$i_{n,out,Rs} = \frac{g_m}{j2\omega_0 C_t} i_{n,Rs} \tag{2.45}$$

$$i_{n,out,Rout} = i_{n,Rout} \tag{2.46}$$

$$i_{n,out,d} = \frac{1}{2} i_{n,d} \tag{2.47}$$

$$i_{n,out,g} = \frac{g_m}{j\omega_0 C_t} \frac{jR_s\omega_0 C_t - 1}{j2R_s\omega_0 C_t} i_{n,g} \tag{2.48}$$

Now the correlation coefficient between $i_{n,g}$ and $i_{n,d}$ is given by Eq. (2.49) [8-9].

$$c = \frac{\overline{i_{n,g} \cdot i_{n,d}^*}}{\sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}}} \tag{2.49}$$

For a long channel device, $c = -0.395j$, and its magnitude decreases as the channel length scales down [5].

The *PSD* of output current due to $i_{n,g}$ and $i_{n,d}$ can be calculated as Eq. (2.50).

$$\overline{i^2_{n,out,\mathrm{g+d}}} = \overline{(A\imath_{n,\mathrm{g}} + B\imath_{n,d})(A\imath_{n,\mathrm{g}} + B\imath_{n,d})^*}$$

$$= |\mathrm{A}|^2 \overline{i^2_{n,\mathrm{g}}} + |\mathrm{B}|^2 \overline{i^2_{n,d}} + AB^* \overline{\imath_{n,\mathrm{g}}.\, \imath^*_{n,\mathrm{d}}} + A^*B \overline{\imath^*_{n,\mathrm{g}}.\, \imath_{n,d}} \qquad (2.50)$$

where, B and A are the transfer function of Eqs. (2.47) and (2.48), respectively.

The last two terms of Eq. (2.50) are output noise due to correlation, and can we obtain by using Eqs. (2.48), (2.49) and (2.5).

$$\overline{i^2_{n,out,\mathrm{c}}} = (jcAB^* - jcA^*B)\sqrt{\overline{i^2_{n,\mathrm{g}}}.\ \overline{i^2_{n,d}}}$$

$$= \frac{g_m.c}{2\omega_0 C_t}\sqrt{\overline{i^2_{n,\mathrm{g}}}.\ \overline{i^2_{n,d}}} \qquad (2.51)$$

By using Eq. (2.44), the total noise factor of cascode topology at ω_0 is calculated as Eq. (2.52).

$$F_{firs\,tstage} = \frac{\overline{i^2_{n,out,Rs}} + \overline{i^2_{n,out,d}} + \overline{i^2_{n,,out,\mathrm{g}}} + \overline{i^2_{n,out,Rout}} + \overline{i^2_{n,,out,\mathrm{c}}}}{\overline{i^2_{n,out,Rs}}} \qquad (2.52)$$

After simplification of Eq. (2.52), we can obtain as Eq. (2.53) to (2.55).

$$F_{first\ stage} = 1 + \frac{g_{g1}(Q^2+\frac{1}{4})P^2\ \frac{g_m^2}{g_{dn}}+\gamma_1\frac{g_{dn}}{4}+\sqrt{\frac{\gamma_1 g_{g1}}{4}}cPg_m+\frac{1}{R_{out}}}{R_S Q^2 g_m^2} \tag{2.53}$$

$$P = \frac{C_{gs}}{C_t} \tag{2.54}$$

$$g_{dn} = \gamma g_{d0} \tag{2.55}$$

The long-channel values for g_{gl} and γ_l are 8/45 and 1, respectively. Parameter P is always less than unity, since C_t is always greater than C_{gs} due to the additional capacitance (C_{ex}).

According to Friis equation, the total noise factor of the designed CMOS LNA is as defined by Eq. (2.56).

$$F_{total} = F_{first-stage} + \frac{F_{subsequent}-1}{G_F} \tag{2.56}$$

where, $F_{first\text{-}stage}$ is the noise factor of the cascode topology, $F_{subsequent}$ is the noise factor of the subsequent stages of LN A, and G_F is gain of first stage of LNA.

Therefore, due to high G_F, the dominant noise source of the LNA is the first stage noise. For this reason, *NF* is minimized at the first stage by using source inductive degeneration and inserting L_x. According to *Eq*. 34, it can be seen that by increasing g_m, F (or *NF* in *dB*) of the first stage can be improved.

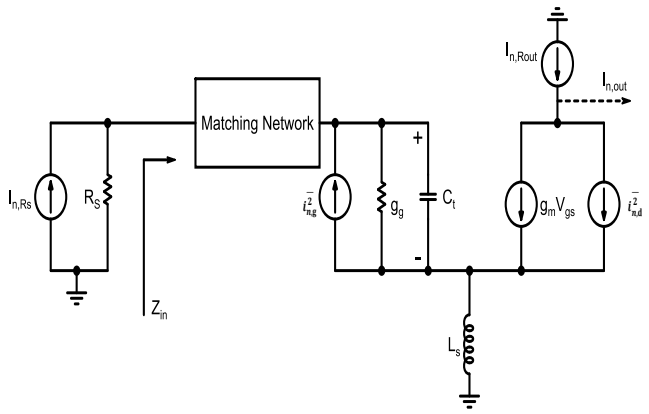


Figure 2.4: Small signal model of a cascode topology with inductively degenerated and noise sources

2.5.4 Sensitivity

The frontend noise figure determines the sensitivity of the overall receiver. This relation is analytically given by Eq. (2.57).

$$\text{Sensitivity(dBm)} = -174\,{}^{\text{dBm}}/_{Hz} + 10\log(BW) + NF_{tot} + 10\log(SNR_{out}) \quad (2.57)$$

where −174dBm/*Hz* is the available noise power from the antenna and BW is the bandwidth of the desired signal, and the last term is the minimum acceptable *SNR* at the receiver output.

As its obvious from (2.17), low NF of the LNA significantly leads to reduce the sensitivity of the whole receiver.

2.6 Linearity

Dynamic range (*DR*) is usually defined as the ratio of the maximum input signal without significant distortion that the circuit can tolerate to the minimum input signal which circuit provides adequate signal quality. Since the input signal of LNA is in the range of nano-volt (nV) or micro-volt (μV), the LNA should possess a large DR to guarantee that it remains linear in the presence of strong distortions. In high frequency, the amplifiers in the receiver chain have to be able to minimize/cancel the adverse effects of large number in-band interferences and inter-modulation/cross-modulation caused by transmitter leakage or blockers. In high frequency amplifiers, nonlinear distortions including inter-modulation, cross-modulation and signal compression may be important and restrict the upper band of DR. However, in low frequency the upper limit of DR is generally defined as maximum input power that the circuit can handle without going into saturation region.

A large in-band blocker tends to desensitize the circuit. It is measured by the 1-dB compression point (P_{1dB}). DR measures the signal handling circuit

capacity, which is limited by the third-order intercept point (*IIP3*) which will explain in details in next section and system noise floor. For high frequency circuits, there are plenty of methods of linearity measurement, but the most common ones are the 1-dB compression point and third-order intercept point.

2.6.1 1-dB Compression Point

The input 1-dB compression point is generally defined as the amplitude of the input/output signal that causes fundamental gain to drop by 1dB from the ideal (or normal) small-signal gain at the specific frequency shown in Figure 2.5. Compression point is considered as an upper bound on the dynamic range of the LNA. Therefore, input signals at the out-of-band of the compression point are usually clipped or saturated at the output.

A nonlinear system can be approximated by using Taylor series described in Eq. (2.58).

$$\mathrm{y(t)} = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots \tag{2.58}$$

The input-referred 1-dB compression point referred in [10] can be calculated as Eq. (2.59).

$$P_{1dB} = \sqrt{0.145 \left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.59}$$

where α_1 and α_3 are the first-order and third-order coefficients of Taylor series expansion.

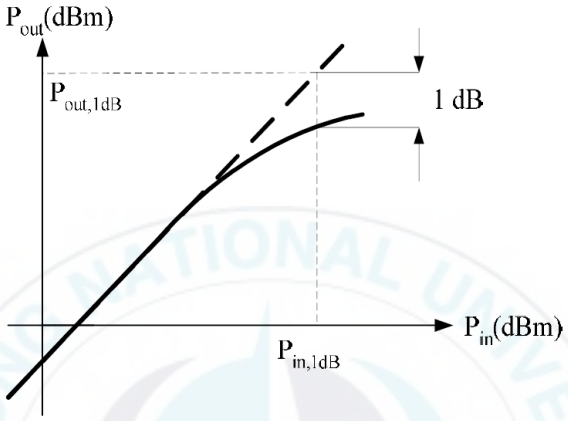


Figure 2.5: 1-dB compression point

2.6.2 Third-order Input Intercept Point (IIP3)

Due to the nonlinear nature of the realistic systems, multiplication of the input signal with its harmonics may cause distortion.

This multiplication leads producing output terms known as inter-modulation products (IMP). For example, if two adjacent sinusoidal signals (also known as "two tones") are feed to the nonlinear system input of an LNA, due to the nonlinearity of the circuit the mixing of the harmonics of

these signals will produce the 2^{nd}- and 3^{rd}- order inter-modulation products at the output and they may lie within the pass band thus, degrading the desired output signal.

To further investigate the effect of inter-modulation, consider a realistic system with the input-output relation given in Eq. (2.58). Now assume that the input signal has the same amplitude but two closely-spaced sinusoidal components as expressed in Eq. (2.60)

$$\mathrm{x(t)} = \mathrm{A}(\cos(\omega_1 \mathrm{t}) + \cos(\omega_2 \mathrm{t})) \tag{2.60}$$

Then at the output of the system, the following terms described in Eqs. (2.61) and (2.62) exist in the vicinity of ω_1 and ω_2.

$$\text{First} - \text{order terms: } \begin{cases} at\ \omega_1 : y_{\omega_1} = \left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3\right)\cos(\omega_1 t) \\ at\ \omega_2 : y_{\omega_2} = \left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3\right)\cos(\omega_2 t) \end{cases} \tag{2.61}$$

$$\text{Third} - \text{order IMP terms: } \begin{cases} at\ 2\omega_1 - \omega_2 : y_{2\omega_1-\omega_2} = \left(\frac{3}{4}\alpha_3 A^3\right)\cos(2\omega_1 - \omega_2)t \\ at\ 2\omega_2 - \omega_1 : y_{2\omega_2-\omega_1} = \left(\frac{3}{4}\alpha_3 A^3\right)\cos(2\omega_1 - \omega_2)\,t \end{cases}$$

(2.62)

The input point that fundamental signal and IMP have the same output power is called third-order input intercept point depicted in Figure 2.6. Mathematically, this can be expressed in Eq. (2.63).

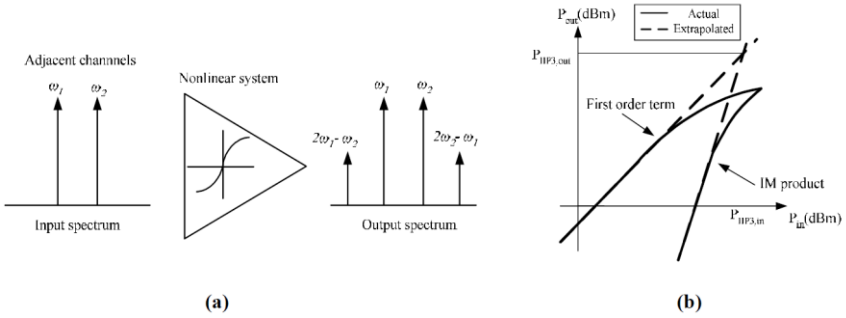


Figure 2.6: (a) Signal spectrum of a nonlinear system and (b) *IIP3* conceptual interpretation

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.63}$$

These calculations are valid if we assume that in $y_{\omega 1}$ and $y_{\omega 2}$ of Eq. (2.62) terms $(\frac{9}{4}\alpha_3 A^3)$ expressions are negligible. However, this assumption no longer holds at the intercept point where the amplitude of signals is quite large. Therefore, the calculated value of *IIP3* in Eq. (2.63) is just an extrapolation of the small input signal.

2.6.3 Linearity Consideration of System Level

Generally a receiver chain consists of several cascaded blocks such as LNA, mixer, VCO etc. Therefore, the overall linearity of a receiver chain

depends on the linearity and gain of each stage. The worst-case *IIP3* of a receiver chain with different gain and *IIP3* of each individual blocks is given as Eq. (2.64) [11].

$$\frac{1}{A_{IIP3,tot}^2} = \frac{1}{A_{IIP3,1}^2} + \frac{\alpha_1^2}{A_{IIP3,2}^2} + \frac{\alpha_1^2\alpha_2^2}{A_{IIP3,3}^2} \tag{2.65}$$

where $A_{IIP3,i}$ and α_i are the *IIP3* and gain of the *i*-th stage, respectively.

A careful examination of Eq. (2.64) reveals that if each stage in a cascade has a gain greater than unity, then the nonlinearity of the following stage becomes more critical [11]. This means that the nonlinearity of stages after LNA, e.g. mixer(s) have the significant effect on the overall nonlinearity rather than the nonlinearity of LNA. This above equation shows that as the LNA gain increases, the linearity degradation is more and more. As we know by increasing the LNA gain, the NF decreases. Therefore, linearity characteristic is in contrast with the NF scenario and there is a trade-off among linearity and NF. Designers typically try to maximize the LNA gain to get a better NF.

2.7 Input Impedance Matching Network

To deliver the maximum power from the antenna to the LNA, the input port of the LNA must be matched to the impedance of antenna, e.g., *50Ω*. For narrowband applications, it's required to match the input impedance of LNA with antenna impedance in a single frequency with very narrow bandwidth. However, for wideband circuits, the impedance matching should be achieved over a wide range of frequency at the LNA input port and is usually a major challenge considering the noise and power consumption requirements.

It is typically to know voltage standing wave ratio (*VSWR*) defined in Eq. (2.6) to measure the degree of the impedance matching [12].

$$\mathrm{VSWR} = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{2.65}$$

where Γ is the reflection coefficient and is defined as Eq. (2.66).

$$\Gamma = \left|\frac{Z-Z_0}{Z+Z_0}\right| \tag{2.66}$$

In this equation, Z_o is the source characteristic impedance, which generally equals to *50Ω* and Z is the actual input impedance. Perfect matching with $Z=Z_o$ results in $\Gamma=0$ *(or* $-\infty$ *dB)* and equivalently *VSWR=1*.

However Γ should be les than -10dB and it's usually sufficient to meet the matching requirement.

2.8 Design Considerations and Analysis

2.8.1 Design Considerations and Analysis

The LNA is a crucial component for radio receivers, and it must meet several requirements such as good input matching, adequate gain and reasonably low noise figure to elevate received signal-to-noise ratio as well as energy-efficiency for battery-powered portable devices [13-14]. In the modern wireless communication systems such as WLAN, UMTS, PCS and 4G LTE, due to the large-scaled interference signals at the input port of the LNA, high linearity is an important requirement for broadband receivers. For narrowband LNA design, one may only need high third-order linearity, while for UWB LNA design we need to consider both the second-order and third-order distortions due to the large numbers of in-band interferences and the cross-modulation/inter-modulation caused by blockers or transmitter leakage [15].

Several techniques have been proposed to achieve high linearity. The pre-distortion method adds a nonlinear element (also called linearizer) prior

to an amplifier such that the combined transfer characteristic of the two devices is linear. In practice, it is impossible to cancel all orders of nonlinearity simultaneously. Therefore, the linearizer is usually designed to cancel the nonlinearity of a certain order. Optimum gate biasing technique is based on the bias condition of the transistors at zero crossing point. The LNA achieves high linearity but the bottlenecks of this technique are that the bias point is bound to change due to the process variations, and the region which this linearity boost can be obtained is very narrow [16].

The feedforward system has been used in many applications because of its unconditionally stable characteristics and ability to provide a broad-band and highly linear amplifier [17-18]. However, the feedforward technique is very sensitive to component tolerance and drift, and it requires adaptive control [18]. Derivative superposition (DS) is the most favourite linearization technique to achieve high linearity [19-20]. The DS is a special case of the feedforward technique. It consists of two parallel transistors. Main transistor operates in the strong inversion region and the auxiliary transistor operates in the weak inversion region. In DS method, by tuning the sizes and bias conditions of the transistors, the third-order nonlinear transconductance coefficient (g_{m3}) can be closed to zero. However, it is not necessary to

completely eliminate the second-order nonlinear transconductance coefficient (g_{m2}) contribution from third-order intermodulation (IM_3). It is noteworthy that since DS method employs multiple transistors in parallel with their gates connected together, it is also called the "multiple gated transistor technique (MGTR)". Since in the DS technique the auxiliary transistor is biased in the triode region, the negative peak magnitude of g_{m3} is much smaller than the positive peak of the main transistor.

Therefore, the proposed LNA can improve both power gain and linearity in high-data-rate standards such as WiMAX and 4G LTE for handsets, and it can be tuned to the desired frequency band. Examples of applications in these ISM bands include radio frequency process heating and medical diathermy machines. The powerful emissions of these devices can create electromagnetic interference and disrupt radio communication using the same frequency, so these devices were limited to certain bands of frequencies. In general, communication equipment operating in these bands must tolerate any interference generated by ISM equipment, and users have no regulatory protection from ISM device operation.

In the proposed MBDS technique a parallel LC tank is used in the emitter of bipolar transistor to reduce the effect of g_{m2} on the third-order input

intercept point. Furthermore, MBDS technique is used in the cascode configuration to further reduce the g_{m2}. By paralleling two capacitances with the gate-to-drain and base-to-collector capacitances of the MOS and bipolar transistors, the phase of g_{m3} can be adjusted respectively, and then the *IIP3* of the whole LNA can be enhanced. The proposed LNA has several applications such as UMTS, PCS and 4G LTE.

2.8.2 Design Considerations and Analysis

2.8.2.1 Fundamentals

In transistors the major factor for nonlinear behavior of the RF blocks is the nonlinear voltage-current relationship, and it is further degraded as the scaling down of the technology. The voltage-current relationship of transistors is expressed as Eq. (2.67).

$$i = g_{m1}v + g_{m2}v^2 + g_{m3}v^3 \tag{2.67}$$

where g_{mi} (i=1,2,3) is the i^{th}-order nonlinear coefficient.

The *IIP3* is the most important parameter for monitoring the linearity performance of the whole LNA circuit and it is expressed as in Eq. (2.63) [18].

Therefore, g_{m3} is the main source of non-linearity in LNAs and by cancelling out it, the linearity can be enhanced. The Taylor expansion series of bipolar transistor can be approximated Eqs. (2.68) and (2.69).

$$i_{CE} = \alpha_1 v_{be} + \alpha_2 v_{be}^2 + \alpha_3 v_{be}^3 \tag{2.68}$$

$$i_{CE} = I_{S0} e^{\frac{V_{BEQ}+v_{be}}{\varphi_t}} = I_{S0} e^{\frac{V_{BEQ}}{\varphi_t}} e^{\frac{v_{be}}{\varphi_t}} = I_Q e^{\frac{v_{be}}{\varphi_t}} \tag{2.69}$$

where V_{BEQ} is the base-to-emitter bias voltage, I_{S0} is saturation current, and φ_t is the thermal voltage. The third-order coefficient can be written as Eq. (2.70).

$$\alpha_3 = \frac{I_Q}{6\varphi_t^3} \tag{2.70}$$

According to Eq. (2.70), α_3 has positive value due to the exponential relationship between the collector current and base-to-emitter voltage. For MOS transistor with negative third-order coefficient the voltage-current relationship is as described in Eqs. (2.71) to (2.74):

$$i_{DS} = \beta_1 v_{gs} + \beta_2 v_{gs}^2 + \beta_3 v_{gs}^3 \tag{2.71}$$

$$i_{DS} = K\frac{x^2}{1+\theta x} \tag{2.72}$$

$$x = 2\eta\phi_t\, Ln(1 + exp(\frac{\mathrm{V_{gs}-V_{th}}}{2\eta\phi_t})) \tag{2.73}$$

$$\beta_3 = -\frac{\theta K}{(1+\theta V_{eff})^4} \tag{2.74}$$

where K =0.5$\mu_o C_{ox} W/L$, μ_0 is the mobility, C_{ox} is the gate capacitance per unit area, θ is the normal field mobility degradation factor, V_{eff} =V_{gs0}-V_{th}, and V_{gs0} is the gate source dc bias voltage.

Figure 2.7 shows schematic of proposed LNA using MBDS technique. As can be seen from Figure 2.7, the bipolar current can be added to the MOS current at the output port to cancel out the g_{m3} of the entire LNA. The output current is expressed as Eq. (2.75).

$$\begin{aligned} i_{out} = i_{DS} + i_{CE} &= (\alpha_1+\beta_1)v_{in} + (\alpha_2+\beta_2)v_{in}^2 + (\alpha_3+\beta_3)v_{in}^3 \\ &= \mathrm{g}_{m1}v_{in} + \mathrm{g}_{m2}v_{in}^2 + \mathrm{g}_{m3}v_{in}^3 \end{aligned} \tag{2.75}$$

From Eq. (2.71) to Eq. (2.75) it appears that the sign of β_3 and α_3 is opposite. To get maximum cancellation of third-order term, the magnitude of β_3 and α_3 must be equal. The third-order term of bipolar transistor is usually more than β_3 of MOS transistor. At the resonance frequency, the emitter LC tank shows a resistance which is used to optimize the value of α_3 and hence

to achieve high linearity. The phase and magnitude of g_{m3} in Eq. (2.75) are dependent on the biasing and the size of the transistors. By tuning the sizes and bias conditions of the transistors, the phase and magnitude of third-order nonlinear transconductance coefficient can be closed to zero.

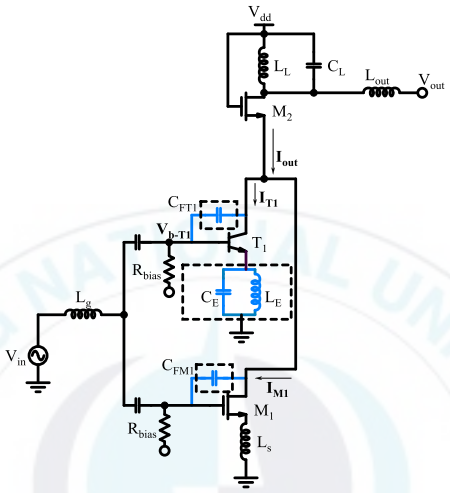


Figure 2.7: Schematic of the proposed LNA

2.8.2.2 Nonlinear Base Capacitance in Bipolar Transistor

Although the bipolar transistor has power-handling capabilities, it has highly nonlinear capacitance at the base junction [9]. This capacitance results in a large second-order harmonic, and it degrades the linearity performance.

A parallel LC tank (L_E, C_E) in Figure 2.7 is used in the emitter of bipolar transistor (T_1) resonating at the second harmonic of fundamental tone to

overcome the degradation of base capacitance. The LC network is employed as source degeneration circuit, and it decreases the current at 4GHz. Since the L_E degenerates the fundamental tone which results in a lower power, the inductor (L_E) should be chosen enough small. The L_E also should be small to have a high quality factor (Q), since the gain does not drop greatly. Thus, the values of the L_E and C_E are chosen to be 0.14nH and 11.2pF, respectively.

The second-order and higher harmonics are simulated with and without the LC tank and the results are shown in Figure 2.8. As shown in Figure 2.8, the LC tank attenuates the high-order harmonics of specially second-order harmonic.

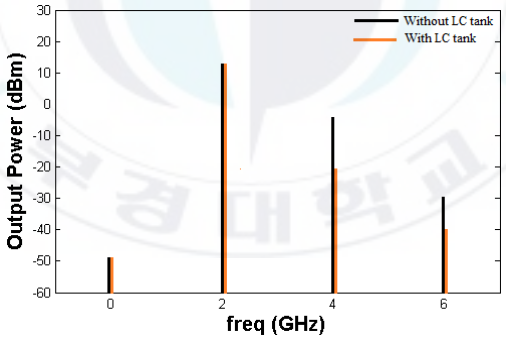


Figure 2.8: Rejection of second-order and higher harmonics of the output power by using LC tank

2.8.2.3 Phase Adjustment by Feedback Capacitances

At high output powers, the nonlinear base-to-emitter capacitance (C_{BE}) of T_1 will change the phase of α_3 and β_3. The linearity performance will be degraded by this phase changing. By adding parallel feedback capacitances the phase of α_3 and β_3 can be adjusted. The values of C_{FM1} and C_{FT1} are 0.55pF and 0.12pF, respectively. Since there is nonlinear capacitance in the base of T_1, the currents i_{T1} and i_{M1} can be expressed as Eqs. (2.76) to (2.80).

$$V_{b-T_1} = \rho_1 v_{in} + \rho_2 v_{in}^2 + \rho_3 v_{in}^3 \tag{2.76}$$

$$i_{T_1} = (v_0 - \rho_1 v_{in} - \rho_2 v_{in}^2 - \rho_3 v_{in}^3) C_{FT1} s + \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3 \tag{2.77}$$

$$i_{M_1} = (v_o - v_{in}) C_{FM1} s + \beta_1 v_{in} + \beta_2 v_{in}^2 + \beta_3 v_{in}^3 \tag{2.78}$$

$$v_o \approx -[(\alpha_1 + \beta_1) R_L] v_{in} \tag{2.79}$$

$$A_{IIP3} = \sqrt{\frac{4}{3}} \left| \frac{j\omega(-(\alpha_1+\beta_1)R_L(C_{FM1}+C_{FT1})-C_{FM1}-\rho_1 C_{FT1})+(\alpha_1+\beta_1)}{-j\omega C_{FT1}\rho_3+\alpha_3+\beta_3} \right| \tag{2.80}$$

where R_L is the resistor at the output port. As shown in Eq. (2.80), the phase difference between α_3 and β_3 can be compensated by using parallel feedback capacitances, and the third-order intermodulation can be cancelled out.

2.8.3 Design Considerations

In a receiver path, since the signal propagates from the antenna to digital backends, different blocks may introduce noise to the signal. The overall *NF* of the receiver depends on the *NF* of each block as well as the gain of preceding stages. Intuitively, larger signals are less susceptible to noise, and this is the reason that the large gain of one stage makes the noise of the following stage less important. Consequently the two major requirements for the LNA performance are low noise figure and high gain. The main contribution of the noise of an LNA is the first stage noise, and so a cascode topology with peaking technique (or shunt technique) is chosen for the proposed LNA to achieve high gain and low noise figure.

The schematic of the whole LNA using MBDS technique is shown in Figure 2.7. The MBDS technique consists of M_1 (MOSFET) and T_1 (BJT). By tuning the width of M_1 (W_1) and bias voltage of transistors, the third-order nonlinear coefficient can be close to zero, and so the *IIP3* can be improved. To achieve good input return loss (S_{11}), series-gate inductor (L_g), source degeneration inductor (L_s) and parasitic capacitances make a LC ladder filter for resonance at the desired frequency. The current-reused topology is one of the suggestions to build an RF front-end, and it minimizes power dissipation

[21-23]. The second stage of M_2 is stacked on top of the first stage to achieve the goal of power saving. At the output, an inductor L_L is placed at the drain primarily for two reasons. The first reason is to resonate with the total drain capacitance to achieve the desired frequency range. The other reason is to provide high enough impedance to allow a good gain [24]. Furthermore, BJTs require less bias current than MOSFETs for the same amount of the third-order intermodulation. Therefore, the BJT contributes a small amount of noise to overall noise of LNA.

2.8.4 Implementation

In an RF circuit, layout plays a very important role in determining the performance of the manufactured chip. Device matching and symmetry, parasitics, current density in interconnects, thermal variations, and substrate effects are the important factors to be considered for doing RF layout [10]. As some important considerations for RF layout, a thick metallization layer should be used for the realization of on chip inductors, and on-chip supply decoupling capacitor should be used to reduce the high frequency noise from the power supply. Manual tiling should be also used to prevent parasitics in critical areas of the circuit.

The commercial software Cadence is used to perform layout and post processing for the low noise amplifier.

The LNAs are fabricated using the 0.18 μm BiCMOS SiGe process. Figures 2.9 and 2.10 show layout and chip micrograph of the 2 GHz LNA, respectively. Post processing has been done for the circuit to verify the true values of parasitics. The values that were extracted from the layout to perform circuit simulation are used. The physical chip area including the pads is approximately 1.2 mm×1.2 mm. The inductor is implemented in the top metal (metal 5), which has a thickness of 10 μm. The input and output pads are laid out in GSG configuration with a pitch of 150 μm to do wafer level testing using a probe station. Signal lines were wide enough to meet electro-migration requirements. Ground lines were made wide to provide low impedance paths. The decoupling capacitor was added to bypass high frequency noise from the bias voltage. Grounded guard ring with substrate connection surrounds the inductor to minimize substrate noise. The MIM capacitors are used for high quality factors and the resistors of Tantalum nitride thin film are used.

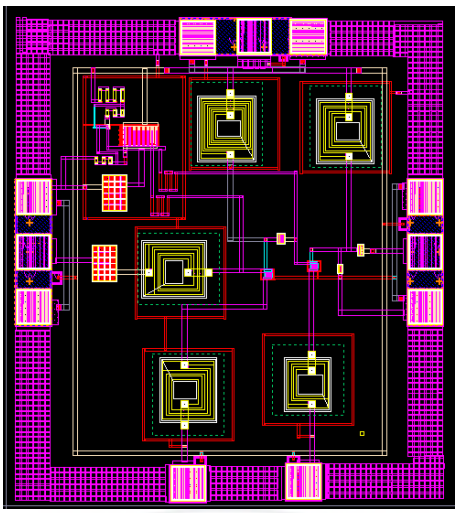


Figure 2.9: Layout of the 2GHz LNA

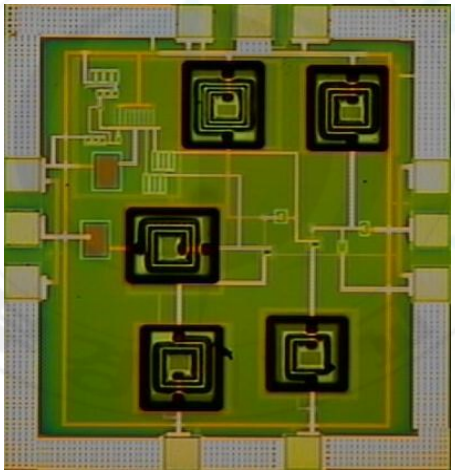


Figure 2.10: Chip micrograph of the 2GHz LNA

2.8.5 Measurement Set-up

This section discusses S-parameter network analyzer measurements for LNA. Vector network analyzers measure the transmission and reflection characteristics of devices and networks by applying a known swept signal from a synthesized source. Device reflection parameters such as reflection coefficient, return loss, VSWR, complex impedance and transmission parameters such as insertion loss and gain can be measured using the instrumentation. Consider the test set-up for S-parameters measurement shown in Figure 2.11.

Figure 2.11: S-parameters measurement set-up

It contains vector network analyzer, wafer probe station, dc power supply, digital multi-meter and PC. The wafer probe station has two RF probes to provide RF input powers at ports 1 and 2 of LNA and two dc probes to provide dc power and ground. The measurements have been used here which represent 2-port measurements. These measured values are translated into LNA specifications such as input impedance, gain, return loss and VSWR using equations in the previous sections.

Figure 2.12 shows on-chip measurements using the wafer probe station. It represents 2-port measurements. Two RF probes are placed at the left and right sides to provide RF input powers at ports 1 and 2 of LNA, and two dc probes are placed at the top and bottom sides to provide dc power and ground. Two RF probes have ground-signal-ground (*GSG*) configuration.

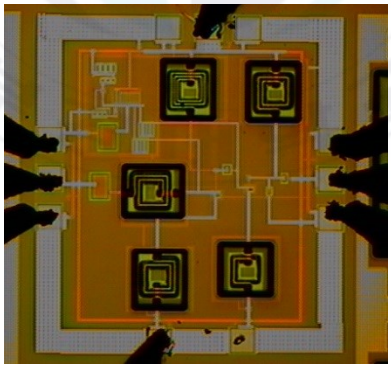


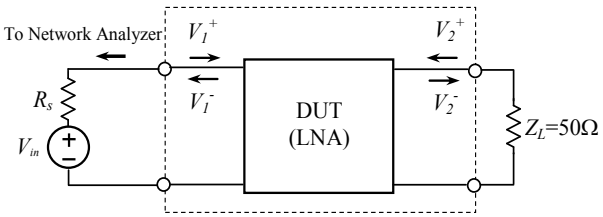
Figure 2.12: On-chip measurement

2.8.6 Experimental Validation

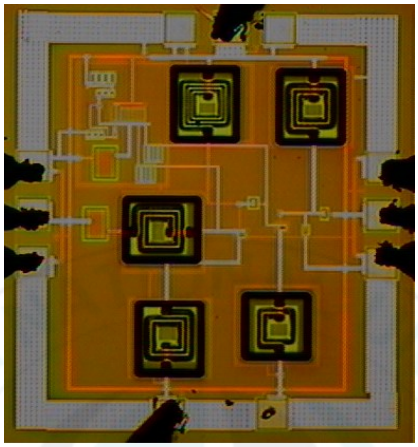
Figure 2.11 shows measurement setup for S-parameter of the LNA. Vector network analyzer and probe station measure the S-parameter by applying a known swept signal from a synthesized source. The S-parameter measurement has been used here which represent 2-port measurements. The powers of -20dBm are applied from the synthesized sources at both port 1 and port 2. We applied the attentions of 0dB at both port 1 and port 2. The measured S-parameter was transferred to voltage gain, return losses and reverse isolation using conventional equations of ADS or MATLAB tool.

Let's consider Figure 2.13 with the source (V_{in}) forming part of a network analyzer with a matched load (Z_L=*50Ω*) at port 2 to measure transfer function (S_{21}) for the LNA. The S_{21} can be obtained by applying an incident wave at port 1, V_1^+, and by measuring the out-coming wave at port 2, V_2^-. This is equivalent to the transmission coefficient from port 1 to port 2. Since S_{21} is a measurement of the gain at the network analyzer output, the transfer function $H(f)$ can be derived to [13].

$$H(f) = S_{21} = \frac{V_2^-}{V_2^+}\Big|_{V_2^+=0} \tag{2.81}$$



(a) Set-up



(b) Die probe

Figure 2.13: Measurement set-up for S-parameter of LNA

2.9 Measurement Results

2.9.1 S-parameter and Noise Figure Measurement

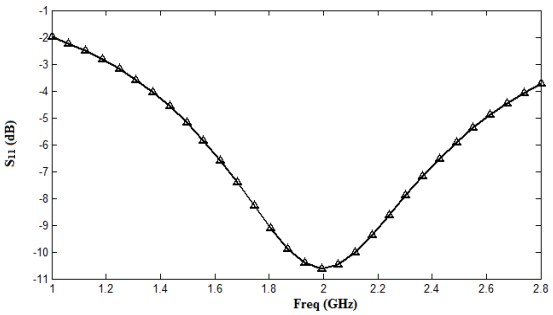
The proposed RF LNA is measured and fabricated in 0.18-μm Si-Ge BiCMOS process. The device dimensions and component values are given in Table 2.1. The linearity performance can be degraded by phase shift. This phase of α_3 and β_3 can be adjusted by adding parallel feedback capacitances.

The values of C_{FM1} and C_{FT1} are 0.55pF and 0.12pF, respectively as shown in Table 2.1. Other values are selected to improve linearity from Eq. (2.80).

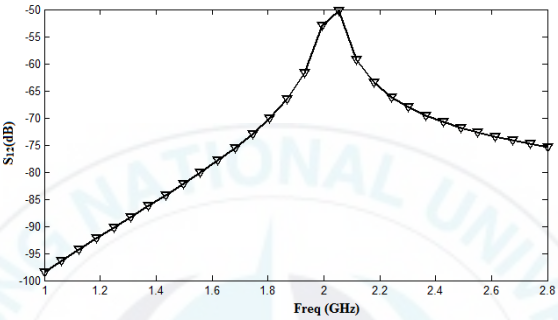
Table 2.1 Aspect ratio of transistors and the value of components

$(W/L)_1$	$(W/L)_2$	C_{FM1}	C_{FT1}	C_E
400μ/0.18μ	268μ/0.18μ	0.55 pF	0.12 pF	11.2 pF
C_L	L_g	L_E	L_L	L_s
4.3pF	6.77nH	0.14 nH	1.36 nH	1 nH

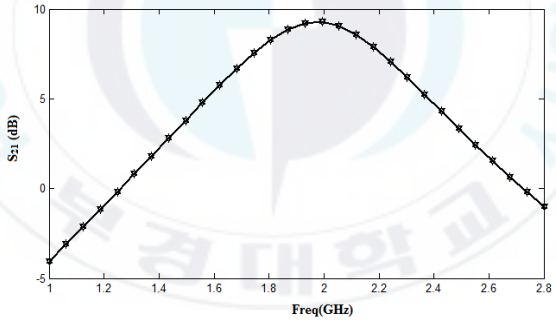
The S-parameter and NF of the proposed LNA is shown in Figure 2.14. The voltage gain (S_{21}) is maximized at 2GHz, while the input return loss (S_{11}) in the frequency of interest is -10.6dB. The circuit showed very small output return loss (S_{22}) of -20.3dB and the excellent reverse isolation (S_{12}) of -50dB. The proposed LNA also showed the very small NF of 2.3dB.



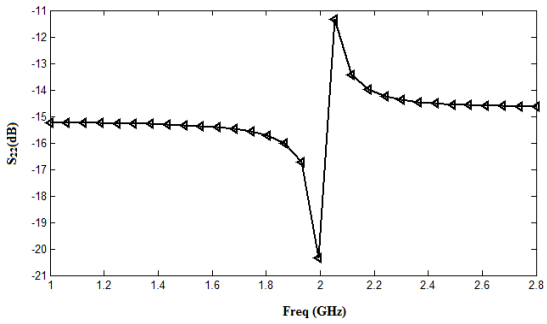
(a) Input return loss (S_{11})



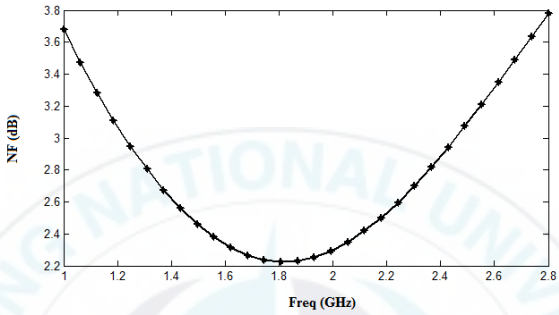
(b) Reverse isolation (S_{12})



(c) Voltage gain (S_{21})



(d) Output return loss (S_{22})



(e) Nose figure

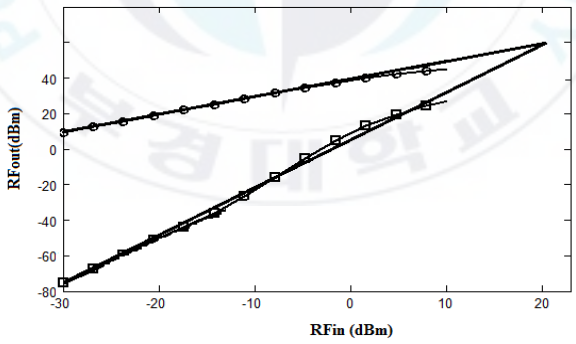
Figure 2.14: S-parameter and noise figure of the LNA

2.9.2 IIP3 and Stability Factor

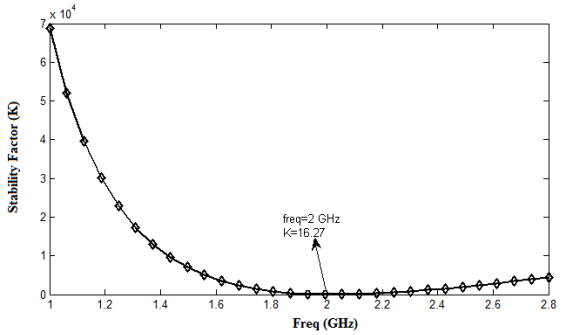
Figure 2.15 shows *IIP3* and stability factor (*K*) of the LNA. Linearity in LNA is typically measured in terms of *IIP3* required to be maximized in [15]. Two-tone test was performed at 2GHz with the spacing of 100MHz. The *IIP3* of the LNA was maximized because of employing MBDS technique and using Eq. (2.80). We analyze the effect of nonlinear capacitances such as

gate-to-source (base-to-emitter) and gate-to-drain (base-to-collector) as well as transcoundactance, g_m (β_F) to improve the linearity. As shown in Figure 2.15(a), the proposed LNA showed the highest *IIP3* of 20dBm as compared to conventional results [3, 19, 20].

In addition to all the major performance parameters, if the circuit operates as expected without undesirable oscillations which could practically destroy the active devices due to the voltage buildup, the stability of the LNA is a basic requirement [15]. The K and $|\Delta|$ are the popular parameters to measure the circuit stability. These values are obtained from Eq. (2.30) [3]. Since the K is greater than unity, and so the LNA is stable at the desired frequency as shown in Figure 2.15(b).



(a) IIP3



(b) Stability factor (K)

Figure 2.15: IIP3 and stability factor of the LNA

The summary of the specifications of the proposed LNA as compared to recently published works is listed in Table 2.2. Using circuit analysis from Eq. (2.80) to achieve high linearity, the main transistor (nMOS) was biased in the strong inversion region while the auxiliary one (BJT) was biased in active region. The MBDS technique can be used to adjust the magnitude and phase of the third-order output current to ensure that they cancel each other out. A LC tank was used in the emitter of bipolar transistor to reduce the second-order nonlinear coefficient which degrades the linearity improvement. Two capacitances were used in parallel with the base-to-collector and gate-to-drain capacitances to adjust the phase of third-order nonlinear coefficient, respectively.

As shown in Table 2.2, the proposed LNA showed the highest *IIP3* of 20dBm as compared to recently reported results. This LNA also exhibited gain of 9.3dB, noise figure of 2.3dB, and power consumption of 5.14mW at the power supply of 1V at 2GHz.

Table 2.2 Comparison of the simulation results of the proposed LNA and other published works

Ref.	**[6][a]**	**[7]**	**[13]**	**[14]**	**This work**
Tech (μm)	0.18	0.13	0.18	0.18	**0.18**
Freq (GHz)	2.1	3.66	2	2	**2**
S21 (dB)	15	14	14.4	26.25	**9.3**
NF (dB)	3	2	1.6	2.2	**2.3**
Power(mW)	10	2.43	0.96	1	**5.14**
IIP3 (dBm)	5	10.5	-9	0	**20**

[a] Measurement Results

2.10. Summary

The two-stage LNA for UMTS and 4G LTE applications was proposed to achieve high linearity by using MBDS technique. This technique was formed by two parallel transistors to improve the linearity performance. We achieved high linearity using the main transistor of nMOS biased in the strong inversion region and the auxiliary bipolar transistor biased in active region. To linearize MOS devices in CMOS technology, the usable possibility of BJT transistor was also explored. The proposed LNA showed excellent *IIP3* of 20dBm as compared to recently reported results. This circuit also showed acceptable voltage gain of 9.3dB, low noise figure of 2.3dB, and low power consumption of 5.14mW at the operation frequency of 2GHz.

3 Design of Low Power and Low Voltage Mixer

3.1 Background

Obviously, downscaling of CMOS technologies has significant impact on the design of analog and radio frequency circuits. Particularly, in low supply voltage circuits, as the technology downscales, the available voltage headroom decreases, and so it makes the designing procedure difficult. Additionally, since the voltage headroom is smaller, the low power consumption in wireless and electronic portable devices and applications is becoming more important. In analog and RF blocks, high output power with high efficiency is desirable, but with the above-mentioned limitations on the recent technologies, achieving these goals requires special attention on the designing circuits with new techniques and topologies.

In the receiver frontend, down conversion mixers are more vulnerable than the other stages due to their configuration. The down conversion mixers are composed of two main stages. As shown in Figure 3.1, the first stage is transconductance, known as G_m-stage, which converts the voltage to current signals for the following stage. The next stage is switching, known as LO-

stage which translates the signal from high frequency to intermediate frequency (*IF*) or to baseband frequency (*BF*).

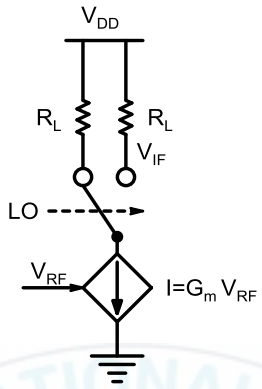


Figure 3.1: Conceptual idea of active mixer

Generally the mixers can be classified in two groups of passive mixers and active mixers. Analysis and description of passive mixers are beyond of concentration this chapter, and only the active mixers will be analyzed. Recently Gilbert-type mixers are widely used due to their reasonable conversion gain, noise figure, and linearity. It should be noted that since mixers are the second block in the receiver chain, linearity, conversion gain and power consumption are the main characteristics.

According to Friis equation, noise figure of LNA is more important than mixer due to the fact that the gain of LNA is normally high which leads

suppressing noise of frontend. Basically, Gilbert cell is stacked on top of the G_m-stage in cascode architecture. As a result, in low supply voltage, low voltage headroom and low power mixer circuits, Gilbert-type is not a good choice.

Several techniques have been proposed for the mixers to operate in the low power supply and low power consumption. In [25], the transconductance and switching stages are decoupled and instead of current source (current commutating) technique, switched transconductance is employed which results in reducing power supply. The other technique is to bias the transistors in the weak inversion region (or subthreshold) [26]. In the subthreshold topology, the ratio of transconducatnce to drain current (I_d) is very high thanks to the fact that drain current is very small and it can be assumed that drain current is in the range of microampere.

As it is noted earlier, the Gilbert cell configures in cascode configuration which increases the supply voltage and supply headroom. To solve this problem, the folded cascode technique has been proposed [27]. However, this architecture suffers from low conversion gain at low supply voltage. The folded cascode technique for biasing RF choke also provides large area in die microphotograph. Folded architecture is susceptible for wideband

applications in mismatch case. At last, it should be noted that, an ideal mixer must have high conversion gain, low power consumption, low supply voltage, low noise and high linearity. It is obvious that there are trade-offs among these features.

3.2 High Linearity Techniques

The increasing demand for wireless communication has resulted in many communication standards. In the broadband systems the receiver chain has to be able to minimize/cancel the adverse effects of large number in-band interferences and inter-modulation/cross-modulation caused by transmitter leakage or blockers. Such an interference minimization/cancellation requires delicate design considerations.

Linearity is the most crucial design specification which plays an important role in RF systems. Special attention has to be paid to the linearity performance of the mixer in a wireless transceiver design. The enhancement in linearity performance should not compromise the desired power/voltage gain or noise figure performance.

Various linearity topologies are reported using different techniques to achieve high linearity. For instance [28] employed optimum biasing (*OB*)

technique to null the main source of nonlinearity (i.e., third-order derivation of transconductance (g_m'')) in common-source (*CS*) without any additional device and used device bias at point which its *IIP3* is maximum. The main bottleneck of OB technique is that the transistor must be biased at ”sweet point”; thus, limiting the tranconductance which leads to reduced gain and increased NF. Feed-forward technique is based on splitting the input into two signals amplified by two amplifiers with different transfer characteristics such that, upon combining their output signals, their distortions cancel each other.

In [29], feedforward technique was exploited in differential pair transistors to improve IIP3 performance. This technique leaded to obtain high linearity, but consumed much power consumption and also degraded the gain and hence, NF. The Derivative Superposition (DS) technique is a special case of the feedforward technique [30]. DS method consists of two parallel transistors. Main transistor works in the strong inversion region and the auxiliary transistor works in the weak inversion region. In DS method, by tuning the sizes and bias conditions of the transistors, g_m'' can be minimized or even canceled. The drawback of this technique is that it is not able to eliminate the second-order nonlinearity coefficient (g_m') which degrades the

IIP3. In DS technique the auxiliary transistor which is biased in the weak inversion region connected to the main transistor and hence, degrades the input matching (due to parasitic capacitances) and NF (due to the gate-induced noise) of whole circuit. To overcome these shortcomings, the modified DS (*MDS*) was proposed in [31]. Additionally, MDS method can eliminate the g'_m in order to achieve high linearity.

In Post-Distortion (*PD*) method [32], not only the auxiliary transistor does not connect directly to the input of the main device, but also connects to the output of the main transistor which minimizes the degradation on the noise figure and input impedance matching.

3.3 Mixer Fundamentals

The mixer is a three port circuit including two inputs known as radio frequency and local oscillator (*LO*) signals, and intermediate frequency at the output port as shown in Fig. 3.2. In the receiver frontend, downconversion mixer is used to translate signals from high frequency to intermediate one. The RF signal comes from the antenna, and it goes to LNA. It also flows into the current source in the G_m-stage, and finally it is converted to the intermediate frequency signal. The IF signal of mixer can be sampled by

analog-to-digital converter (*ADC*) a filter can be placed between the mixer and ADC which results in enhancing linearity and noise to eliminated the spurious and noise spectrum.

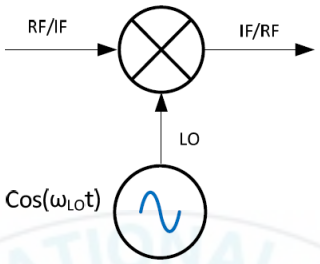


Figure 3.2: Mixer symbol

Mixers are used to translate the frequency must be either time varying or nonlinear since time-invariant systems cannot generate output signals with spectral components that are not available in the input port. There are diverse techniques to realize mixing operation but the main idea for the different topologies lies in the multiplying two signals in the time domain or lies in convolusion of the desired signal with the impulse train the frequency domain. With this assumption that the two signals are $A_1cos(\omega_1 t)$ and $A_2cos(\omega_2 t)$, the multiplication is given as Eq. (3.1).

$$A_1 \cos(\omega_1 t)\, A_2 \cos(\omega_2 t) = \frac{A_1 A_2}{2}[\cos(\omega_1 t - \omega_2 t) + \cos(\omega_1 t + \omega_2 t)] \quad (3.1)$$

It is obvious from Eq. (3.1) that two input signals provide the phase of summation and difference and the amplitude of two signals results in of the multiplication of each amplitude.

3.4 Main Characteristics of Mixers

3.4.1 Conversion Gain

The conversion gain can be expressed in two methods such as voltage conversion gain or power conversion gain. The power conversion gain is defined as the ratio of the available power deliver to the load at the output frequency to the available power at the input frequency which can be written as Eq. (3.2).

$$\mathrm{CG} = 10\log\frac{available\ power\ at\ the\ output\ frequency}{available\ power\ at\ the\ input\ frequency} \quad (3.2)$$

The voltage conversion gain is defined as rms value of output signal to the rms value of input signal as described in Eq. (3.3).

$$G_{V,dB} = 20\log(\frac{V_{IF}}{V_{RF}}) \quad (3.3a)$$

$$G_{VP,dB} = 10\log(\frac{P_{IF}}{P_{RF}}) = 10\log(\frac{\frac{V_{IF}^2}{R_{IF}}}{\frac{V_{RF}^2}{R_{RF}}}) \quad (3.3b)$$

3.4.2 Local Oscillator Power

Voltage-controlled oscillator (VCO)[1] is basically utilized to generate local oscillator signals. However phase-locked loop (PLL) also can be used to produce LO signals, but it needs several circuits, and it occupies much more space in the layout and fabrication chip. LO signals are used in switching stage of mixer circuits to fully make the transistors on or off to reach the maximum gain in the system. As shown in Figure 3.3, it is desired to reach the highest conversion gain while using as low as LO power (P_{LO}) especially in low power applications. As it will be discussed in next chapter among receiver frontend blocks, VCO has the highest power consumption. Thus, to reduce VCO power consumption, low P_{LO} is required to turn on and off the transistors in the switch stage.

[1] VCO analysis is presented in Chapter 4.

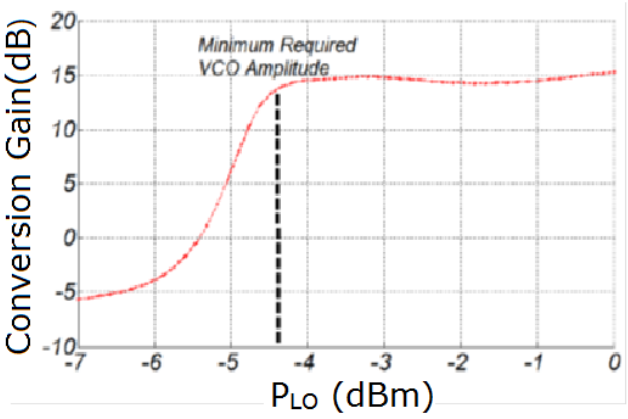


Figure 3.3: Conversion gain versus amplitude of LO

3.4.3 Noise Figure

Noise figure is not as simple as other blocks, and hence it is so confusing. As shown in Figure 3.4, there are three noise sources at the output port (*IF*) as follows:

1. The noise at RF band which down converts to IF
2. The noise at image RF band which down converts to IF
3. The noise of mixer circuit due to the use of passive and active elements

Therefore, in summary, at IF frequency both image and wanted (or desired) signals which down convert by mixers can be found.

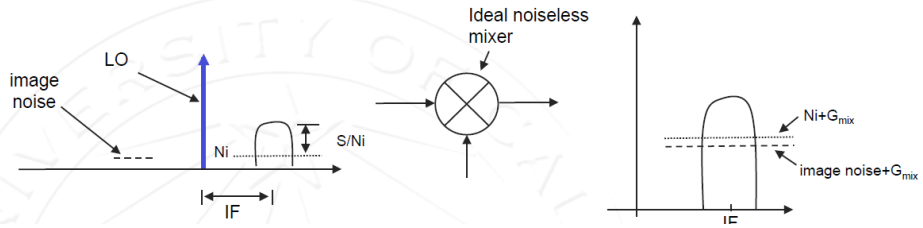


Figure 3.4: Noise sources in mixer

There are two definitions for noise figure: single-side band (*SSB*) and double-side band (*DSB*).

Single-side band NF is defined when the source of noise in the image band is only source noise, and image signal is suppressed by the filters after mixer. In other words, the output noise degradation is only due to the noise source and it is independent of image signal which defined as Eq. (3.4).

$$\frac{S_{out}}{N_{out}} = \frac{S_d}{2N_d+2N_{mix}} = \frac{S_d}{N_d}\left[\frac{1}{2+\frac{2N_{mix}}{N_d}}\right] \tag{3.4a}$$

$$F_{SSB} = 2 + \frac{2N_{mix}}{N_d} \tag{3.4b}$$

where S_{out} is the desired output signal, S_d is the desired signal, N_d is noise in the desired band, and N_{mix} is the noise in the image band.

The double-side band NF is defined by this assumption that the image band includes both the noise and image signal. The DSB NF is as Eq. (3.5).

$$\frac{S_{out}}{N_{out}} = \frac{2S_d}{2N_d+2N_{mix}} = \frac{S_d}{N_d}\left[\frac{1}{1+\frac{N_{mix}}{N_d}}\right] \quad (3.5a)$$

$$F_{DSB} = 1 + \frac{2N_{mix}}{N_d} \quad (3.5b)$$

3.4.4 Port to Port Isolation

In mixer, the amount of feedthrough from one port to the other port is known as isolation which in ideal mixer it is desired to be infinity. However in practical port, isolation between mixer ports is finite due to the parasitic capacitances in transistors at high frequency and port to port path as shown in Figure 3.5. Among different port to port isolations, the feedthrough from LO to IF (*LO-IF*) and from RF to IF (*RF-IF*) are important. The additional leakage to the output would cause additional components in the IF port. Furthermore, any leakage to input would make additional modulation and it results in widening the frequency response. To solve the isolation problem, output bandpass filters (*BPF*) are the favorable solution. The filters in the *IF* ports would filter out the unwanted spectral terms.

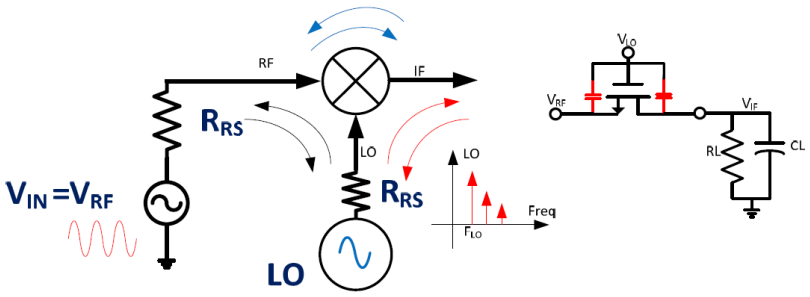


Figure 3.5: Different port to port leakages in mixer

3.5 Active Mixer Architecture

With accordance to mixing method of RF and LO signals, there are three types of mixers known as unbalanced, single-balanced, and double-balanced.

3.5.1 Unbalanced Mixer

The schematic of the unbalanced mixer is illustrated in Figure 3.6 including G_m-stage and switching stage. As it is clear from Figure 3.6, since there is only one output, this configuration is called unbalanced mixer. The function of G_m-stage is to covert the voltage signal to current one as simple common source configuration. As explained earlier, the switching stage translates signals from radio frequency into intermediate frequency using switching operation in a period of time. The output voltage and conversion

gain of the single-balanced mixer after simplification is expressed in Eq. (3.6) and (3.7).

$$V_{out} = I_{out}R_L = I_{RF}\,S(t)R_L$$
$$= R_L(I_{DC} + G_m V_{RF})(S_0 + S_1\cos(\omega_{LO}\mathrm{t}) + S_2\cos(2\omega_{LO}\mathrm{t}) + \cdots) \quad (3.6)$$
$$= R_L(I_{DC} + G_m V_{RF})(\tfrac{1}{2} + \tfrac{2}{\pi}\cos(\omega_{LO}\mathrm{t}) + \tfrac{2}{3\pi}\cos(3\omega_{LO}\mathrm{t}))$$

$$\mathrm{CG} = \frac{|V_{IF}|}{|V_{RF}|} = \frac{G_m R_L}{\pi} \quad (3.7)$$

where V_{out} is the output voltage, I_{out} is the output current, R_L is the load resistor, and $S(t)$ is the switching pulse train, I_{DC} is the dc current of current source, V_{RF} is the input voltage of Gm-stage, and G_m is the transconductance of the current source transistor.

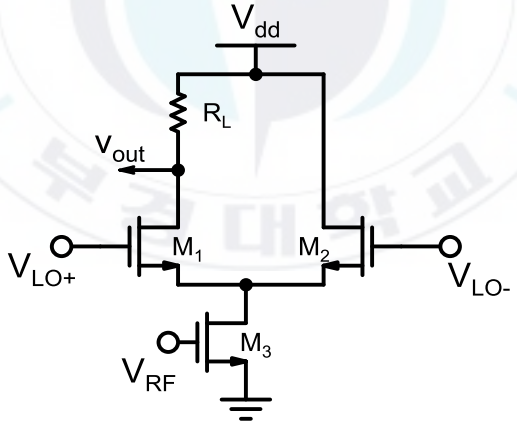


Figure 3.6: Unbalanced mixer schematic

3.5.2 Single-Balanced Mixer

The major problems of unbalanced mixer are low isolation and conversion gain. To solve these problems and enhance the performance of the mixers, single-balanced mixer is depicted in Figure 3.7. As can be seen, since the output is differential, normally single-balanced mixer's conversion gain is double of unbalanced mixer with single output. Better conversion gain results in enhancement of noise figure ae well. Additionally, the differential output leads to reduce/eliminate the output dc offset due to the both switching and transconductance stages. Therefore, in single-balanced mixer, the output offset is less than the previous one.

The output voltage and conversion gain of this mixer is expressed in Eq. (3.8) and (3.9).

$$\begin{aligned} V_{out} &= I_{RF}(S\left(t - \tfrac{T_{LO}}{2}\right) - S(t))R_L = I_{RF}\, S(t)R_L \\ &= R_L(I_{DC} + G_m V_{RF})(2S_1\cos(\omega_{LO}\mathrm{t}) + 2S_2\cos(3\omega_{LO}\mathrm{t}) + \cdots) \\ &= R_L(I_{DC} + G_m V_{RF})(\tfrac{4}{\pi}\cos(\omega_{LO}\mathrm{t}) + \tfrac{8}{3\pi}\cos(3\omega_{LO}\mathrm{t})) \end{aligned} \tag{3.8}$$

$$\mathrm{CG} = \frac{|V_{IF}|}{|V_{RF}|} = \frac{2G_m R_L}{\pi} \tag{3.9}$$

By considering the effect of input matching network and by assumption that the switches are not ideal (rising and falling times (τ_{sw}) are not zero), the conversion gain is expressed in Eq. (3.10).

$$\mathrm{CG} = \left(\frac{Z_m}{Z_{RS}+Z_m}\cdot\alpha_m\right).\left(\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\right).\left(\frac{g_{m2}}{\sqrt{g_{m2}^2+\omega^2 C_T^2}}\right).\left(\frac{2R_{L-max}g_{m3}}{\pi}\right) \tag{3.10}$$

where α_m represents the transfer function from matching input network toward the current source (G_m-stage). T_{sw} and T_{LO} are the switching time and LO signal period, respectively.

The switching time is function of dc bias current LO power and the size of transistors in the switching stage and is expressed as Eq. (3.11).

$$T_{sw} = T_{sw}(P_{LO}, I_{DC}, SW\ size) \tag{3.11}$$

The port isolation can be also expressed as expressed as Eq. (3.12) to (3.14).

$$V_{out} = R_L(I_{DC} + G_m V_{RF})(\frac{4}{\pi}\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\cos(\omega_{LO}\mathrm{t}) + \cdots) \tag{3.12}$$

$$V_{LO-IF} = \frac{4}{\pi}R_L I_{DC}\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\cos(\omega_{LO}\mathrm{t}) \tag{3.13}$$

$$V_{RF-IF} = 0 \tag{3.14}$$

As it is proved, in single balanced mixer the input port is absolutely decoupled from the output port which is an advantage for this architecture in comparison with the previous one that suffer from port feedthrough problem.

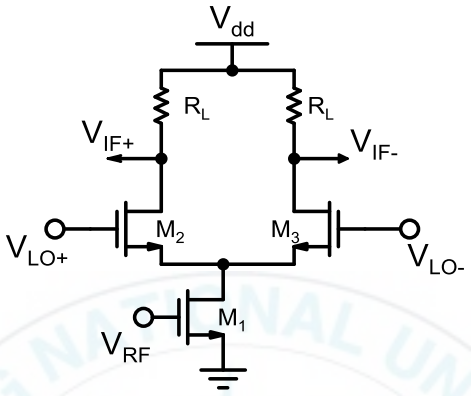


Figure 3.7: Single-balanced mixer schematic

3.5.3 Double-Balanced Mixer

To improve conversion gain and isolation issues of single-balanced mixer, double-balanced mixer is shown in Figure 3.8. In simple words, the double-balanced mixers are composed of two single-balanced mixers in fully differential architecture. Conversion gain of double-balanced mixer has double gain in comparison with single-balanced mixer and the LO leakage at the output port will be cancelled out. However, these enhancements provide high power consumption. As it pointed earlier, since the double-balanced

mixer contains two single-balanced, double-balanced mixer has double power consumption in comparison with single-balanced mixer.

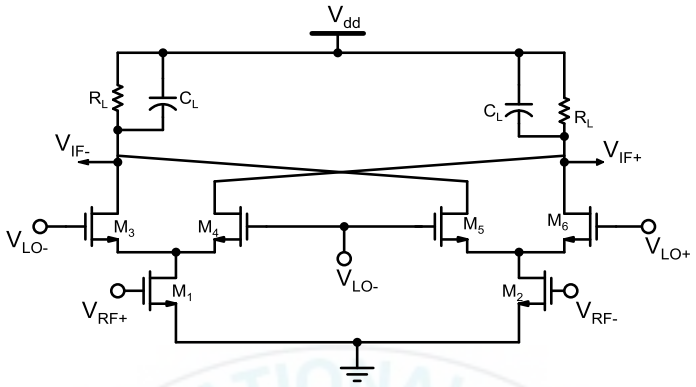


Figure 3.8: Double-balanced mixer schematic

The conversion gain of double-balanced mixer is presented in Eq. (3.15).

$$\mathrm{CG} = \frac{|V_{IF}|}{|V_{RF}|} = \frac{4G_m R_L}{\pi} \tag{3.15}$$

Similar to Eq. (3.10), by considering the effect of input matching network and by assumption that the switches are not ideal, the conversion gain is also described as Eq. (3.16).

$$\mathrm{CG} = \left(\frac{Z_m}{Z_{RS}+Z_m} \cdot \alpha_m\right).\left(\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\right)\left(\frac{g_{m2}}{\sqrt{g_{m2}^2+\omega^2 C_T^2}}\right)\left(\frac{4R_{L-max}g_{m3}}{\pi}\right) \tag{3.16}$$

The port to port isolations are listed in Eq. (3.17) to (3.19).

$$V_{out} = 2R_L(I_{DC} + G_m V_{RF})(\frac{4}{\pi}\text{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\cos(\omega_{LO}\text{t}) + \cdots) \quad (3.17)$$

$$V_{LO-IF} = 0 \quad (3.18)$$

$$V_{RF-IF} = 0 \quad (3.19)$$

It is clear that the double-balanced mixer significantly enhances the isolation among different ports due to its unique structure.

3.6 Design Considerations and Analysis

3.6.1 Mixer Description

Power consumption and linearity are the most crucial characteristics of downconversion mixers. It is desired to design circuits with low supply voltage and low power consumption and high linearity. According to Eq. (3.20), for achieving high linearity, first-order transconductance (g_{m1}) has to be as high as possible. In addition, the g_{m1} has proportional relationship with gate-source voltage (V_{gs}) and V_{gs} in proportional with drain current (I_d). Therefore, it can be concluded that as linearity is high, the drain current and hence power consumption is high. Thus, there is a severe tradeoff between power consumption and linearity.

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{3.20}$$

For the sake of having high linearity with low power consumption simultaneously, a new circuit has to be designed. In this section the new idea will be presented and analyzed to fulfill the above-mentioned tradeoff. Note that the new operates in the low power supply. Finally, the simulation results of the proposed mixer circuits will be shown to verify the feasibility of the new idea.

3.6.2 Mixer Analysis

The simplified schematic diagram of conventional I/Q mixer is shown in Figure 3.9 (a). It is composed of two cascased mixers, and each mixer consists of voltage to current (V-I) converter, Gilbert cell and current to voltage (*I-V*) converter. As can be seen the V-I converter converts the applied input voltage to current which is steered by the first mixer switch. The first mixer converts the high frequency current signal to IF signal. Then the translated signal at the output of the first mixer is reconverted to voltage by the I-V converter. The second V-I converter, also converts the IF voltage to current for the chopping function. The second Gilbert cell mixer converts

IF current signal to baseband one, and ultimately the second I-V converter converts the steered current to voltage at the output port. High power consumption and low linearity are bottlenecks of this traditional architecture. The former comes from cascode structure in the first and second stages, and the latter is due to the existence of I-V and V-I converters.

Figure 3.9(b) illustrates the proposed mixer to alleviate drawbacks of the conventional architecture. Firstly, to avoid selection of cascode topology, a folded structure has been chosen. Folded mixers have become popular structure for high linearity and low voltage operation. It is possible to avoid stacking transistors with a folded mixer [33]. However, folding the circuit adds additional current branches. By utilizing folded structure, the voltage headroom will be also increased. Furthermore, the first V-I converter is deleted and replaced by a complementary push-pull (CPP) topology which functions as an LNA to increase the linearity and gain.

Secondly, the first mixer is realized using pMOS transistor. The pMOS switches in LO stage help mixer to achieve same overdrive voltage and consequently similar linearity performance with lower power consumption as compared to the case of nMOS transistors [34].

Finally, the first and the second I-V converting trans-resistor are realized in resistor to avoid employing inductor which leads to occupy large die area. Moreover, the second V-I converter is removed and this causes the double balanced mixer connects directly to the first switch mixer.

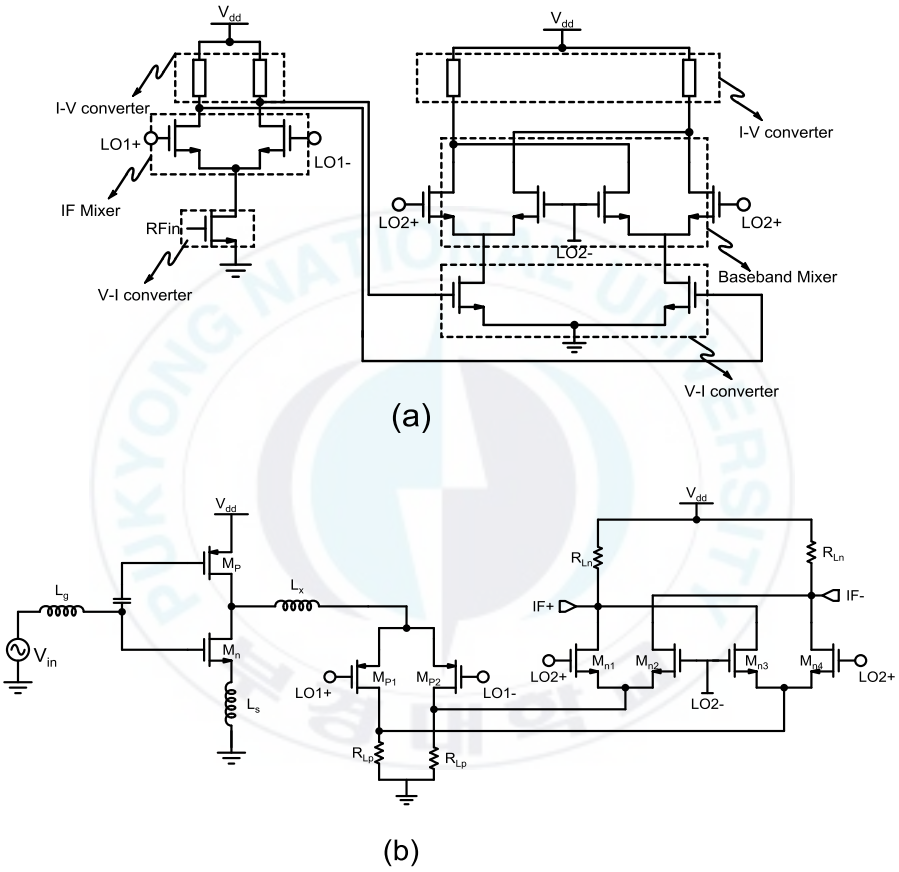


Figure 3.9: (a) Conventional mixer with two stage and (b) proposed mixer using folded architecture

Low power consumption and low voltage operation are two essential requirements for mixers. Low voltage mixers are challengeable because traditional mixers rely on stacking multiple transistors [35]. In addition, circuits designed with MOS transistors biased in subthreshold region operate on lower voltage headroom resulting in smaller power supply and further reduced dc power dissipation [36]. Thus, the proposed mixer switches are biased in subthreshold region to reduce the power consumption. Furthermore, Figure 3.10 clearly depicts that by biasing the switch transistors in weak inversion region, a gain enhancement of 10 dB will be yielded in comparison with biasing in strong inversion region.

There is another benefit to operate the mixer transistors in subthreshold inversion region. With this assumption that all switch transistors have constant transconductance in subthreshold inversion the noise performance will be significantly improved as compared to strong inversion. There are two types of noise in RF frontend. Firstly, flicker noise which is inversely proportional to transistor size, and a weakly inverted transistor will be considerably larger than a strongly inverted transistor. Secondly, thermal noise will be reduced because the value of the drain thermal noise factor (γ) is approximately 25% smaller in weak inversion [37]. Meanwhile, in

subthreshold region the required LO signal power is expected to be smaller, and so it leads to reduce the dc power consumption of LO signal generator.

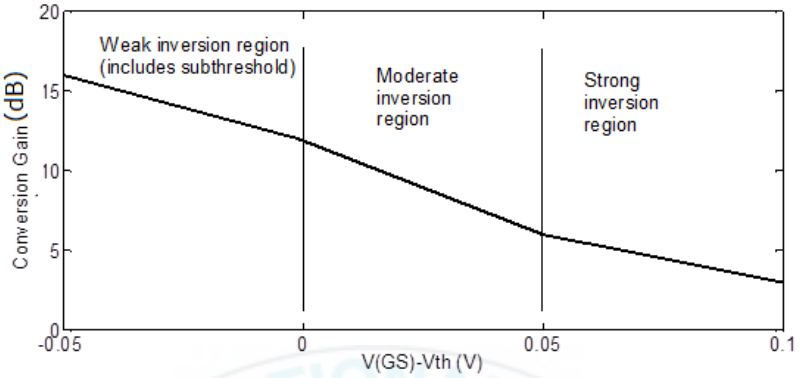


Figure 3.10: Conversion gain versus mixer transistor regions

3.6.3 Results and Discussions

To verify the validity of the proposed mixer, the mixer is implemented in 130-nm CMOS process. The transistors in the switching stages are biased in the subthreshold regime to reduce power consumption. At the supply voltage of 1V, the power consumption is 3.11mA. It should be noted that in the proposed folded cascode mixer, the G_m-stage (current-source) is deleted and in place of it, and LNA is utilized. Therefore, the power consumption of Mixer and LNA is only 3.11mA. The conversion gain of the mixer is

depicted in Figure 3.11. As can be seen from the figure, the maximum power gain at 24GHz is 19.6dB.

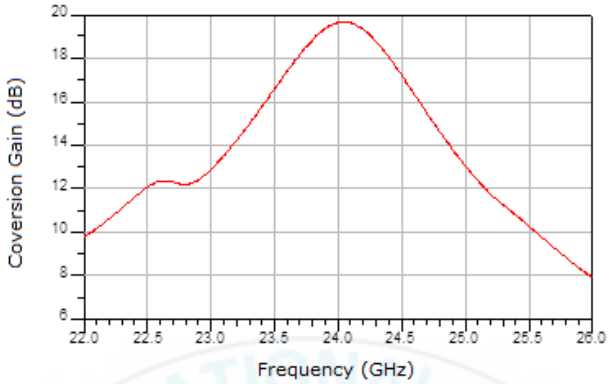


Figure 3.11: Conversion gain versus frequency

Mixer suffer from high noise due to the different noise sources such as noise in image band, noise in the desired band, and noise of passive and active device. The noise figure of the proposed mixer is shown in Figure 3.12.

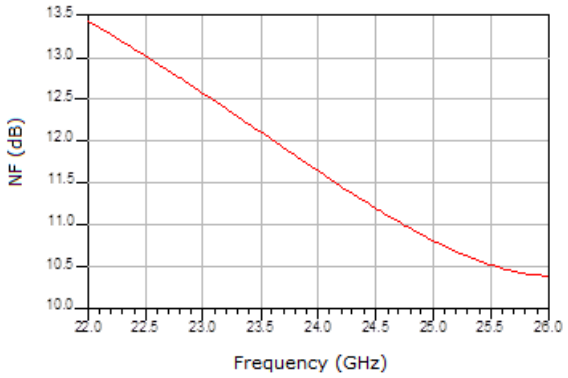
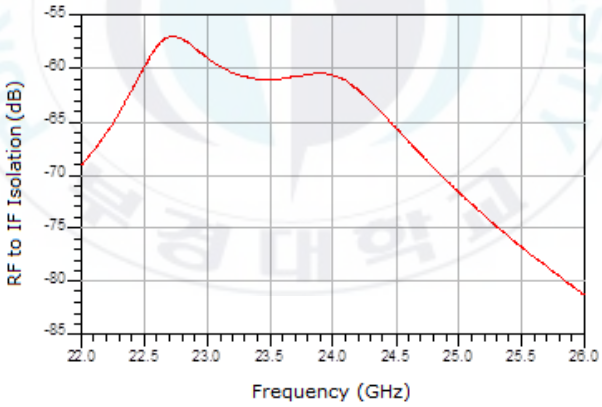
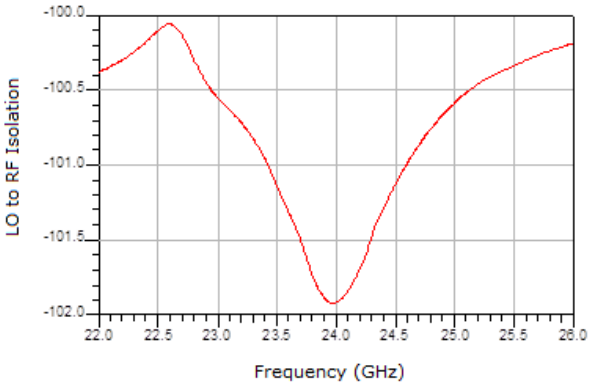


Figure 3.12: Noise figure versus frequency

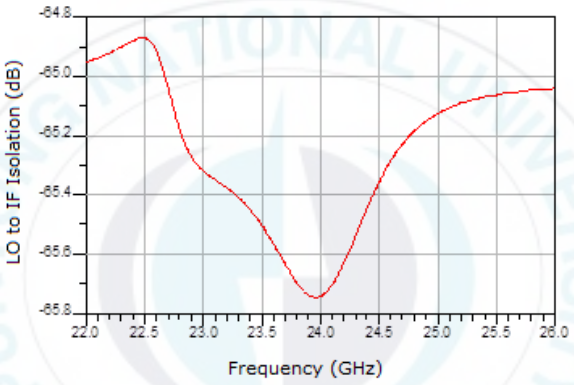
In the proposed mixer, due to its unique structure, the feedthroughs among different sources are very low that can be neglected. The port to port isolations are illustrated in Figure 3.13.



(a) RF to IF isolatioin.



(b) LO to RF isolatioin.



(c) LO to IF isolatioin.

Figure 3.13: Different port to port isolation versus frequency

Figure 3.14 shows the conversion gain versus the LO power. It is desired to reach the conversion gain peak at the low LO power due to the fact that VCO needs low power consumption to generate the sine wave signal to switch the transistors on and off. As it is clear the required LO power is -1dB.

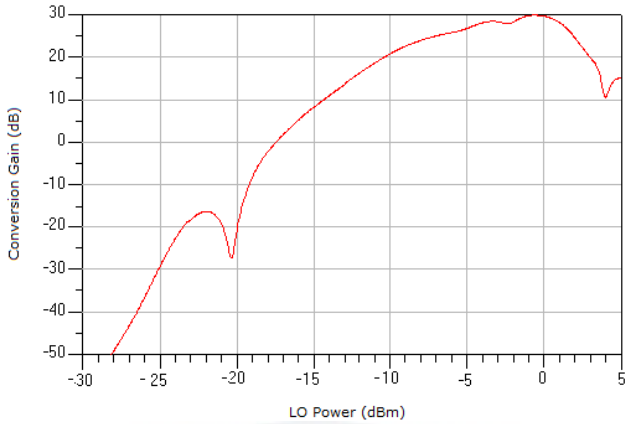


Figure 3.14: Conversion gain versus LO power

3.7 Summary

A cascode folded mixer is proposed to reduce the supply voltage and power consumption. In the proposed mixer, the G_m-stage has been removed to reduce the supply voltage and increase the voltage headroom. The transistors in the switching stage are biased in the subthreshold to reduce the power consumption as well. In the cascode folded structure, the LNA is placed instead of current source in Gm-stage to increase the conversion gain and hence reduce the noise figure. And finally, by utilizing the new mixer, excellent port to port isolations have been achieved.

4 Design of Voltage Controlled Oscillator

4.1 Background

The design and implementation of single-chip transceivers have already been demonstrated in CMOS technologies for RF CMOS integrated circuits (*ICs*). For wireless communication circuits, voltage-controlled oscillators (*VCOs*) are one of the transceivers key elements. Oscillator is an independent circuit, since some self-sustaining mechanism generates a periodic stable sinusoidal signal. VCO also can be used as a part of the frequency synthesizer to produce the local oscillator signal for both downconversion and upconversion mixers. Oscillation can be sustained by providing the system with an appropriate amount of positive feedback or negative resistance that can compensate any loss in the circuit as shown in Figure 4.1. Due to the better relative phase noise performance of inductance-capacitance, (*LC*) tank oscillators are preferred to ring oscillators for monolithic integration in CMOS technology. Beside the limitations in the applied semiconductor technology an ideal VCO should meet most of these specification such as low phase noise, low power, wide tuning range, high integration, small die area accuracy and low cost.

The ring oscillator is classified as a waveform oscillator and it displays advantages such as high integration in VLSI and wide tuning range, and small chip area. Usually, it generates lower frequencies than the LC tank ones, so this feature leads reducing the large pre-scaler requirement or frequency dividers that occupy much space and contribute to their own noise.

LC oscillators achieve lower phase noise in comparison with ring ones for a given power consumption. Thus, LC VCOs are often preferred for higher frequencies with low power and low phase noise. One obvious disadvantage of LC VCO is to use an/more inductor(s) and often variable capacitors to control the tuning voltage which occupy large area on the chip. Therefore, LC VCOs are not well-suited for VLSI implementation.

The phase noise characteristics of LC tank VCOs at low power supplies are superior to that of the ring oscillators, and as the technology is being further downscaled, this feature is becoming increasingly crucial [38]. For the applied tuning and the resulting output frequency, the frequency tuning characteristics of the ring oscillator display a fairly linear behaviour [39]. However, at lower power supplies, as the phase noise becomes more dominant, the linearity suffers more and more.

Varactors, variable reactors, or voltage controlled capacitors based on MOS structure are widely used as tuneable capacitors in LC VCOs, and their capacitance features define the output oscillator frequency.

Also, it's hard to predict the output of VCOs because large amplitude swings at the LC VCO output impact the effective capacitance of the varactor modulating the output frequency. When a varactor with abrupt capacitance characteristics is used in an LC VCO, and the oscillator amplitude swing is directly applied across it, the frequency curve shows strong dependence on the bias current (I_{bias}). Distortion is also introduced by the bias current and the oscillation sustaining active elements and it corrupts the output frequency curve by the upconversion of various noise sources to the resonance frequency.

The other factors that severely reduce the capacitance tuning range are parasitic capacitances of tank inductor, the drain overlap capacitances, wiring and gate to source capacitances.

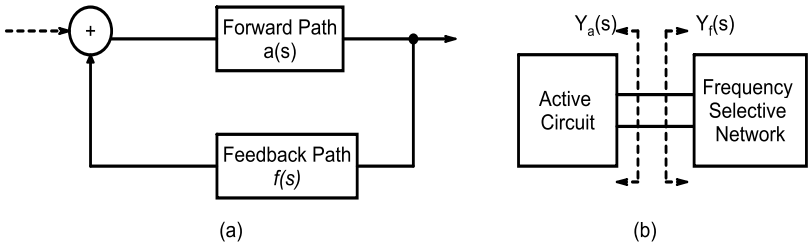


Figure 4.1: (a) Feedback model, and (b) negative resistance model

4.2 Start-up Considerations

Consider an oscillator as a linear feedback system as shown in Figure 4.1(a). To ensure start-up case in oscillators, the loop gain ($T\ (j\omega)$) must fulfill the following necessary but not sufficient conditions as described in Eq. (4.1).

$$\angle \mathrm{T}(\mathrm{j}\omega_y) = 0, \quad |T(\mathrm{j}\omega_y)| > 1 \tag{4.1}$$

where ω_y is the frequency at the total phase shift of zero through forward and feedback paths.

In other words, to ensure start-up, loop gain should be at least one or equivalently a minimum amount of negative resistance is required. A small signal model of a generalized LC oscillator during start-up is illustrated in Figure 4.2.

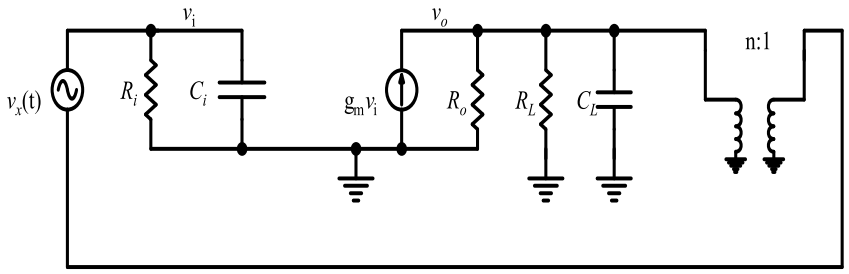


Figure 4.2: Small signal LC oscillator model

The circuit shown in Figure 4.2 which assumes a unilateral device has transfer function [40] described in Eq. (4.2).

$$\frac{v_o(s)}{v_i(s)} = \frac{s.g_m L}{1+\frac{sL}{R_T}.(1-A_l)+s^2 LC} \tag{4.2}$$

where $A_l = \frac{g_m R_T}{n}, R_T = R_o \parallel R_L \parallel n^2 R_i$ and $C = C_L + {C_i}/{n^2}$. The poles of transfer function are expressed in Eq (4.3) and (4.4).

$$s_1, s_2 = -\left(\frac{1-A_l}{2R_T C}\right) \mp \sqrt{\frac{1}{LC} - \left(\frac{1-A_l}{2R_T C}\right)^2} \tag{4.3}$$

$$|s_1| = |s_2| = \sqrt{\frac{1}{LC}} = \omega_0 \tag{4.4}$$

Figure 4.3 transfer function for different values of loop gain. As the loop gain (A_l) changes poles s_1 and s_2 move a across the complex plane perfect circle. The effects of varying A_l are shown in Figure 4.3.

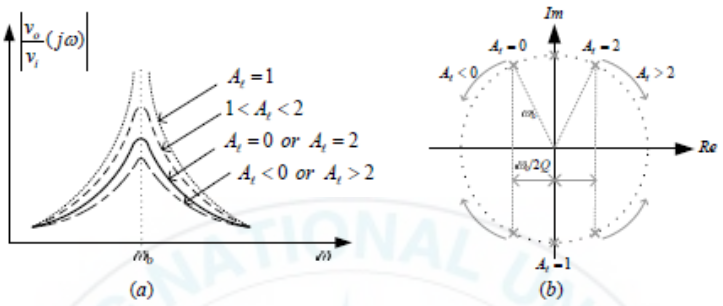


Figure 4.3: (a) Magnitudes (b) root Lucas of transfer function for different values of loop gain

Under nominal conditions, practical A_l is equal to 3-5 to guarantee oscillation start-up at all operating temperatures and under worst case process variations. Although linear feedback methods were taken but for negative resistance an equivalent criterion may be reached. Differential VCO topologies are very common in today's communication systems; therefore, the above analysis is also applicable to them.

Figure 4.4 shows an extensively used differential VCO topology, where start-up criteria are evaluated using both negative resistance and feedback methods. In Figure 4.4, R_a is the equivalent resistance looking into the differential cross-couple pair of MOS transistors. R_f is the equivalent differential resistance of the frequency selective network including both LC tanks and R_T is the each LC tank equivalent resistor. The g_m is the small signal transconductance of either M_1 or M_2. Each approach results in the same start-up criterion.

Negative resistance approach is expressed in Eq. (4.5a) to (4.5d).

$$\frac{1}{R_a} + \frac{1}{R_f} \leq 0 \tag{4.5a}$$

$$R_a = -\frac{2}{g_m} \tag{4.5b}$$

$$R_f = 2.R_T \tag{4.5c}$$

$$g_m \geq {}^{1}/_{R_T} \tag{4.5d}$$

Feedback approach is also described in Eq. (4.6a) to (4.6b).

$$A_l \geq 0 \tag{4.6a}$$

$$A_l = (g_m R_T)^2 \geq 1 \tag{4.6b}$$

$$g_m \geq {}^{1}/_{R_T} \tag{4.6c}$$

This criterion determines the basic lower limit on power consumption and has a direct impact on the design process.

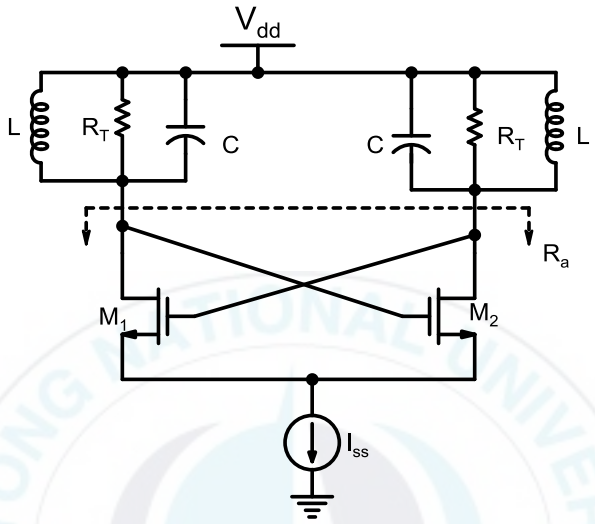


Figure 4.4: Start-up requirements of cross-coupled LC VCO

4.3 Steady-state Considerations

Due to some excitation, for v_x(t) (see Figure 4.2) in two-pole transfer function given in Eq. (4.2), the natural and forced response of v_o(t) can be achieved as Eq. (4.7).

$$v_o(t) = f\big(v_x(t)\big) + A_1.e^{-\frac{\omega_0}{2Q}(1-A_l)}\cos(\omega_0' t) \tag{4.7}$$

where A_1 depends on initial conditions and ω_0' is the frequency of zero-crossing during oscillation build-up (the imaginary term of Eq. (4.7)) and is close but not equal to the steady-state frequency of oscillation ω_0.

The coefficient of second term in Eq. (4.7) grows exponentially for $A_1 > 1$. Steady-state is eventually reached in VCO where the exponential nature of $v_o(t)$ brings the oscillator into a nonlinear region of operation as depicted in Figure 4.5. In steady-state, there are two characteristics. Firstly, the poles of oscillator transfer functions are positioned almost exactly on top of the imaginary axis providing the phase of two poles of zero. Secondly, the loop gain also approaches unity.

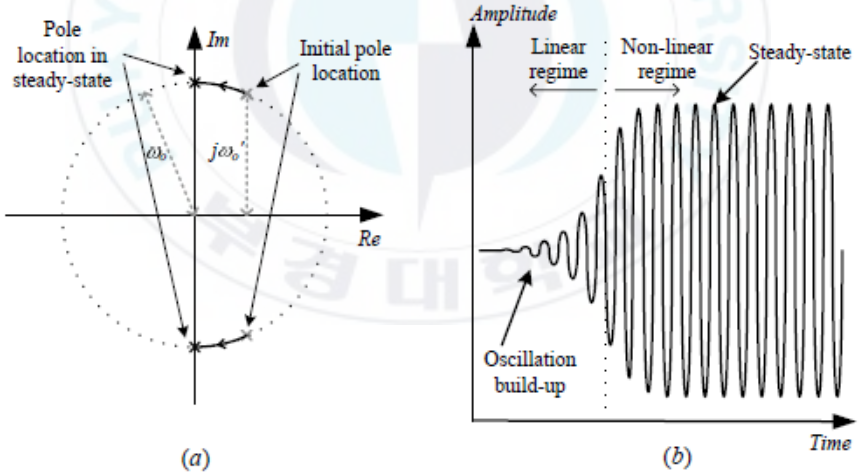


Figure 4.5: (a) Root Locus of LC oscillator and (b) LC oscillator output

waveform

4.4 Phase Noise in LC Oscillators

The accurate phase noise analysis of LC oscillators is complicated and time-consuming to give useful design insights. We assume LC VCO as a linear time-invariant (*LTI*) system to reach a basic understanding for phase noise.

4.4.1 Linear Time-Invariant Phase Noise Analysis

The generic LC oscillator with uncorrelated noise sources $\overline{i_{n,1}^2}$, $\overline{i_{n,2}^2}$ and , $\overline{v_{n,1}^2}$ from the active device is illustrated in Figure 4.6. The circuit is treated as a positive feedback amplifier with a loop gain very close to but less than unity.

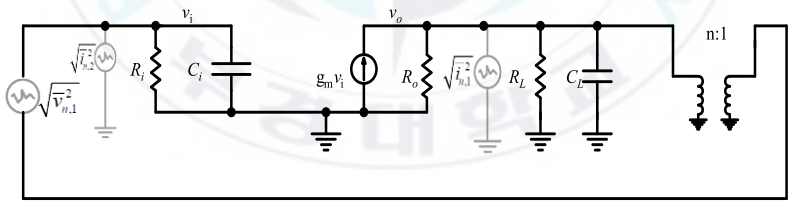


Figure 4.6: Noise sources in LC VCO schematic

For simplicity, all noise sources are written by a single equivalent noise generator as expressed in Eq. (4.8).

$$\overline{i_n^2} = \overline{i_{n,1}^2} + \frac{\overline{i_{n,2}^2}}{n^2} + \overline{v_{n,1}^2}\left(G_m - \frac{1}{nZ_i}\right)^2 + 4k_B T \frac{1}{R_L}\Delta f \tag{4.8}$$

where Z_i is the input impedance of active device (transistor), k_B is Boltzman's constant, and the last term is made by thermal noise from R_L. In Eq. (4.8), G_m is transconductance of the device, and it could be a small-signal or large-signal quantity.

The output voltage noise can be calculated as Eq. (4.9).

$$\sqrt{\frac{\overline{v_o^2}}{\Delta F}} = -\frac{\sqrt{\frac{\overline{i_n^2}}{\Delta f}} \cdot Z_T}{1 - G_m \frac{Z_T}{n}} \tag{4.9}$$

where Z_T is the loaded tank impedance and at frequency offsets its relatively close to the carrier. It is approximated as Eq. (4.10).

$$Z_T \approx \frac{R_T}{1 + 2jQ_0 \frac{\omega - \omega_0}{\omega_0}} \tag{4.10}$$

By substituting Eq. (4.10) into Eq. (4.9), we obtain.

$$\frac{\overline{v_o^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot \left(\frac{R_T^2}{(1-G_m\frac{R_T}{n})^2+4Q_0^2(\Delta\omega/\omega_0)^2}\right) \tag{4.11}$$

where $\Delta\omega = \omega - \omega_0$.

The first term of the denominator in Eq. (4.11) in steady-state regime, at $\Delta\omega$, becomes negligible due to the device limitation and decrease of the loop gain. Therefore, the normalization of Eq. (4.11) is given in Eq. (4.12).

$$\frac{\frac{\overline{v_o^2}}{\Delta f}}{V_0^2}(\Delta\omega) \approx \frac{\frac{\overline{v_n^2}}{\Delta f}}{V_0^2} \cdot \frac{1}{4Q_0^2\,(\frac{\Delta\omega}{\omega_0})^2} \tag{4.12}$$

where $\overline{v_n^2} = \overline{i_n^2} \cdot R_T^2$.

For the LC VCO shown in Figure 4.6, the LTI approximation of the single-sided noise spectral density, known as phase noise is described in Eq, (4.13).

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\frac{1}{2} \cdot \frac{\frac{\overline{v_n^2}}{\Delta f}}{V_0^2} \cdot \left(\frac{\omega_0}{2Q_0\Delta\omega}\right)^2\right] \tag{4.13}$$

4.4.2 Linear Periodically Time Varying (LPVT) Phase Noise Analysis

Obviously, in steady-state region the oscillator operates in a nonlinear regime and its operating point is periodically time-varying. Since the transistor bias point is periodically time-varying, its noise generators are not stationery. However, noise probabilities due to the tank losses are stationary.

Despite the fact that an oscillator operates nonlinearly, they showed that its noise-to-phase transfer function is itself linear. By considering the periodically time-varying behavior of this linear relationship they established a new quantity, namely the (phase) impulse sensitivity function (*ISF*). The ISF describes a charge input to excess phase output transfer function vs. launch time, or, because of its periodicity, vs. the phase angle of the oscillation cycle. Noise generators inject charge disturbances from different points of the circuit. Hence, the ISF must be evaluated at each relevant node. A periodically time varying impulse response can be defined as in Eq. (4.41) [4].

$$h_{\emptyset}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} \cdot u(t-\tau) \tag{4.14}$$

where *u(t)* is the unit step function. In order to make $h_\phi(\mathrm{t},\tau)$ independent of amplitude, $\Gamma(\omega_0\tau)$ is normalized to the q_{max} (maximum charge swing) across the capacitor.

The excess phase due to a small current disturbance at node x, $i_x(\tau)$ is then given by Eq. (4.15).

$$\emptyset_x(t) = \int_{-\infty}^{\infty} h_{\emptyset,x}(t,\tau)\cdot i_x(\tau)\cdot d\tau \tag{4.15}$$

To calculate the net phase noise, the contributions of all noise sources in the circuit must be taken into account. The equivalent white noise current generator can make the following phase noise as described in Eq. (4.16).

$$\mathcal{L}\{\Delta\omega\} = 10.\log\left[\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right] \tag{4.16}$$

where $\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi}|\Gamma(x)|^2 dx.$

The cyclostationarity of a given noise source can be handled using an effective ISF and expressing the noise source itself as being stationary, as

explained in [41]. To compare the phase noise of LTI system with LPVT one, we substitute $q_{max} = CV_{max} = \sqrt{2}CV_0$ into (4.16), and we obtain Eq. (4.17).

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\frac{1}{4}\frac{\overline{i_n^2}/\Delta f}{V_0^2}\frac{\Gamma_{rms}^2}{C^2}\cdot\left(\frac{1}{\Delta\omega}\right)^2\right] \quad (4.17)$$

The main limitation of the LPVT analysis is that determining *Γ(x)* requires cumbersome simulations. Since today's simulation CAD tools (e.g. SpectreRF) are able to compute phase noise directly, it is not common practice to compute *Γ(x)* separately.

4.5 LC VCO Topologies

The LC VCO topologies implemented from single cross-coupled configurations that display less noise and increased robustness [42], to more sophisticated ones, such as the noise shifting Colpitts oscillator taking into consideration the current waveforms as well as timing of the voltage to enhance energy transfer efficiency, and hence reducing phase noise [43].

Single cross-couple configuration can be designed in both tail-biased cross-coupled and top-biased cross-coupled. The core of most of LC VCO topologies are often the same including the resonance tank and active devise (MOS, bipolar transistors and etc.) and, but with modifications for specific

applications. According to the application, the designers can tune the elements to gain the specific characteristics. In this section two types of cross-coupled topologies will be explained in details.

4.5.1 Single Cross-Coupled LC VCO Topology

In the single cross-coupled LC VCO shown in Figure 4.7(a), input of each transistor in differential configuration is connected to the output of the opposite transistor resulting in the negative resistance. Due to the ease of implementation, relative good phase noise, relaxed start up conditions and differential operation, this topology is extensively employed in high frequency integrated circuits.

As working with other blocks in a typical radio frontend, differential operation significantly suppresses the sensitivity of circuit to undesired common mode disturbances from other blocks sharing the same substrate. This structure also rejects supply, substrate noise amplification, and upconversion effect between current source and active devices.

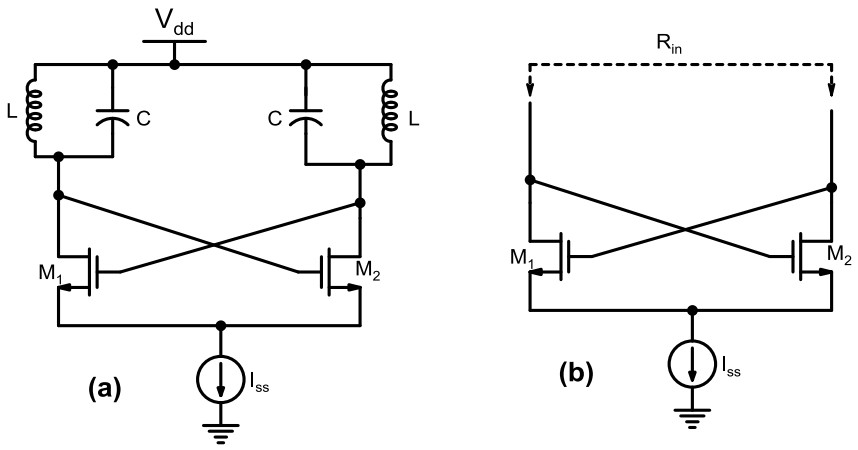


Figure 4.7: Single cross-coupled LC VCO

As shown in Figure 4.7(a), for this oscillator the current source is placed at the source terminals of MOS transistor of tail-biased cross-coupled scheme. However the current source can be inserted at the drain terminals of transistor of top-biased cross-coupled scheme, to reduce the sensitivity and variations in the supply voltage. Since the pMOS transistor itself has lower noise feature than the nMOS one, the single cross-coupled differential topology also may be implemented in pMOS pair [44]. On the contrary, at lower frequencies the pMOS cross-coupled pairs provide negative resistance, but at higher frequencies, it acts as an active load rather than a negative resistance [45]. The negative resistance can be seen at the drains of M_1 and

M_2, and it is expressed as $R_{in} = -2/g_m$ as shown in Figure 4.7 (b). Furthermore, R_{in} must compensate the losses of inductors, capacitors and MOS parasitics to make the circuit oscillate.

At either V_O^+ or V_O^- of the VCO the tank voltage (V_{tank}) is the single-ended peak-to-peak voltage swing and it is given by Eq. (4.18).

$$V_{tank} \approx \frac{2}{\pi} I_{bias} R_P \tag{4.18}$$

where R_p is the effective tank parallel.

4.5.2 Complementary Cross-Coupled LC VCO Topology

A complementary cross-coupled topology consists of both nMOS and pMOS transistors as shown in Figure 4.8 which leads providing more positive gain [46]. The increased current that flows through both the pMOS and nMOS devices results to higher power efficiency. The negative resistance in complementary configuration is twice as large as the single pair relaxing the start-up criteria. Moreover, in the complementary cross-coupled pair, the large oscillation signals V_O^+ and V_O^- isolate between V_{dd} and ground reducing the coupling of the signal to the power supplies. The total negative resistance of the complementary LC VCO is given as Eq. (4.19).

$$R_{negative,total} = R_{inn} \parallel R_{inp} = -\frac{2}{g_{m1}+g_{m34}}. \quad (4.19)$$

Assuming that the current in the differential stage switches quickly from one side to the other, hence at high frequency of operation, the V_{tank} can be obtained as Eq. (4.20) [48].

$$V_{tank} \approx I_{bias}R_P \quad (4.20)$$

The importance of increased Q-factor of the LC-tank is apparent as it translates to a larger effective tank parallel resistance R_p, this allows a lower oscillator bias current, while maintaining a large voltage swing, without clipping the signal amplitude at V_{dd}. Operating with less bias current while maintaining the same amplitude, will result in improved phase noise performance. Although it should be considered that in the complementary coupled LC VCO case, since the pMOS pair increasingly consumes voltage headroom, so even if the nMOS pairs power consumption is reused, the total power is not necessarily reduced. In addition, adding a pMOS pair will introduce extra flicker noise, and so the improvement in the phase noise may be negligible [45].

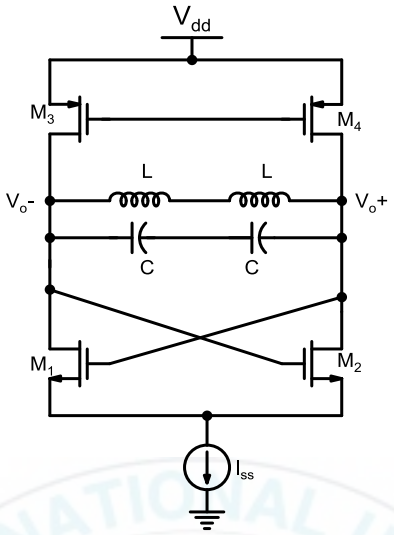


Figure 4.8: Complementary cross-coupled LC VCO

4.6 Design Trade-offs

LC VCO performance can be evaluated by several parameters such as frequency tuning range, phase noise oscillation frequency, power dissipation, and power supply. In the oscillator the association of the design variables, such as total tank capacitance, inductor parameter, width (W) and length (L) of the transistors, and bias current results in a large number of methods to enhance VCO performance. Due to limitations on the Q-factor of inductor, its design has received a lot of attention [47].

This section briefly explains design trade-offs among the phase noise and power consumption. According to semi-empirical phase noise model of Leesons in Eq. (4.20), when the oscillator signal swing is maximized the phase noise performance is better [49].

$$\mathcal{L}\{\Delta\omega\} \propto \frac{N}{P_s Q_L}\left(\frac{\omega_c}{\Delta\omega}\right)^2 \tag{4.21}$$

where N is the noise factor, P_s is the signal power at the resonator, Q_L is the quality factor of the resonator with all the loading in place, ω_c is the oscillating frequency and $\Delta\omega$ is an offset frequency from the carrier.

As the output frequency of oscillator is influenced by amplitude variations, when the oscillator is operating in the current limited region, it is dependent on the bias current [50]. In the current-limited region according to Eq. (4.22), the oscillator amplitude V_{tank} linearly increases with the bias current, until the oscillator enters the voltage limited region [48].

In the voltage-limited region, the MOS transistor enters into saturation region and hence, the supply voltage is maximized and constant. Thus, in this region, there is an upper limit for the supply voltage and growth of amplitude tank. When the oscillator enters into this region, the tank amplitude no longer

grows with the bias current. Therefore, any further increase in the bias current via increasing supply voltage or width/length of transistor will result in a waste of power. V_{tank} according to these two regions of operation is expressed in Eq. (4.22) as shown in Figure 4.9:

$$V_{tank} = \begin{cases} \frac{I_{bias}}{g_{tank}}, & (I - limited) \\ V_{limit}, & (V - limited). \end{cases} \tag{4.22}$$

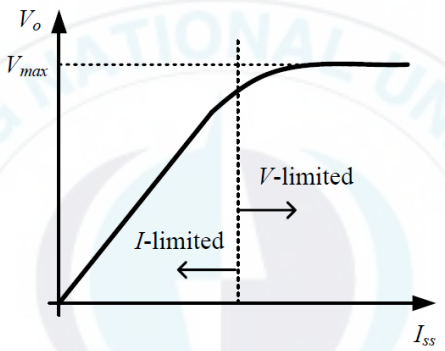


Figure 4.9: Voltage amplitude versus I_{ss} for typical LC VCO in steady-state mode

For typical LC VCOs, the best trade-off among power consumption and phase noise is biasing the MOS transistors at the border between the current- and voltage- limited regions. Also, as the VCO amplitude swing is boosted, the SNR ratio will increase, and the effect of on the thermal noise sources will be less. However, with larger amplitude swings, we can utilize the

variable capacitor. Therefore, there will be increased in the amplitude to frequency modulation which resulting in increasing sideband phase noise.

4.7 VCO Description

Nowadays, one of the serious global concerns is road traffic crashes. To enhance safety, automotive radar devices are now installing on many transport and luxury passenger vehicles. Automotive radars are utilized in advanced cruise control (*ACC*) systems, which can provide information for driver, and activate the accelerator of vehicle's motor and brakes to check and control the distance between two cars. Radar-based driver assistance systems also have other important functions such as collision warning systems, blind-spot monitoring, lane-change assistance, rear cross-traffic alerts and back-up parking assistance, collision mitigation systems and vulnerable road user detection. The main frequency bands of radar applications are 24GHz as well as 77GHz. For the sake of detection other near vehicles in the medium-short range and wide beam, 24GHz is the mainstream.

Recently with the downscaling of CMOS technology, implementation of highly integrated low phase noise, low voltage and low power dissipation

voltage controlled oscillators is one of the major challenges in the radio frequency frontend modules. Among the various types of oscillators, LC VCO has been widely used thanks to its better phase noise at low supply voltage and its relaxed and reliable start-up mode. In the battery-driven systems, local oscillator still consumes a large portion of the current in the frontend. Thus, low phase noise and low power dissipation are two of crucial concerns in designing procedure of VCO to reduce bit error rate (*BER*) and to increase the battery life-span.

The CMOS technology benefits from the merits of high system level integration capability and low fabrication cost, but it suffers from the intrinsically low transconductance and higher flicker noise at the corner frequency. Unfortunately, at high frequencies the low transconductance of MOS transistor makes it difficult to design low power transceivers specifically VCOs. Different circuit topologies and methodologies have been proposed to overcome those limitations [52-53].

One of the promising approaches is utilizing cascode current-reuse [54] configuration in the designing procedure. High gain, relatively high bandwidth, and high stability are the most important features of cascode arrangement. Since in the cascode structure, two MOS transistors are stacked

on top of the other one, it needs high supply voltage resulting in high power consumption. To overcome this bottleneck, current-reuse technique is used to reduce power consumption. Thus, cascode current-reuse structure has low power consumption which is the most important characteristic of radar sensors in the car industry.

In this study, a cascode current-reuse structure is utilized to simultaneously reduce the power consumption and increase the transconductance and gain of the VCO circuit. The capacitive-feedback technique [55] including two series capacitors is also used to improve voltage swing of output ports under low power and low supply voltage conditions. Besides, by employing the VCO varactors in the capacitive-feedback technique, an extensively wide oscillation frequency tuning range is achieved. Frequency dependent negative resistor technique is employed in parallel with inductors to enhance the symmetry and phase noise of oscillator within the frequency band.

4.8 Proposed Current-reuse LC VCO

The proposed VCO is shown in Figure 4.10. The tail current-shaping transistor in conventional cross-coupled LC VCO [56] is replaced by inductor to reduce the power supply and eliminate the pertinent noise resulting in high phase noise. The capacitive-feedback technique including C_1 and C_2 is utilized to enhance the output swing of LC VCO. The composition of on-chip inductors and capacitors in the capacitive-feedback technique cause the drain voltage of pMOS swings above the supply voltage (V_{dd}) and the source voltage of nMOS swings below the ground (*zero*), respectively. Since the varactors in the proposed current-reuse LC VCO are utilized in parallel with source terminals, a small change on their values leads to a large variation in the frequency. Furthermore, the proposed circuit shows a reasonable phase noise thanks to employing cascode current-reuse structure and elimination of current-shaping source.

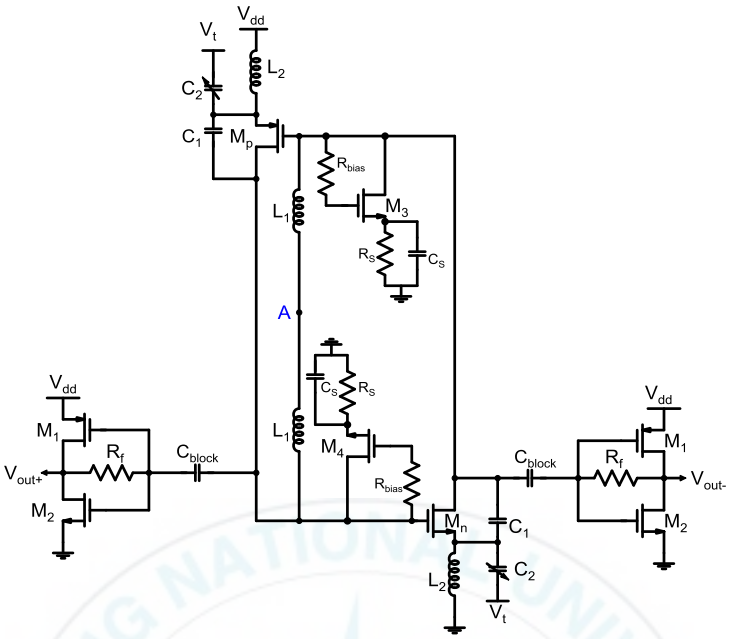


Figure 4.10: The proposed current-reuse LC VCO with capacitive-feedback technique

4.8.1 Start-up Considerations

The half-circuit equivalent small-signal without negative resistance of the proposed current-reuse LC VCO is illustrated in Figure 4.11. Inductors L_1 and L_2 are the LC tank inductors with R_{P1} and R_{P2} losses, respectively. The parasitic capacitances of the transistors smaller than the C_1 and C_2 are neglected. The current-reuse topology provides a center-tab node A, shown

in Figure 4.10, where is placed between two inductors L_1. Since the n/pMOS transistors operate in the differential mode, the center-tab node functions as a virtual ground and hence it simplifies the DC self-biasing and high frequency analysis. For the sake of simplicity in the calculation the losses of the inductors are assumed to be parallel with inductors as shown in Eq. (4.23) and Eq. (4.24).

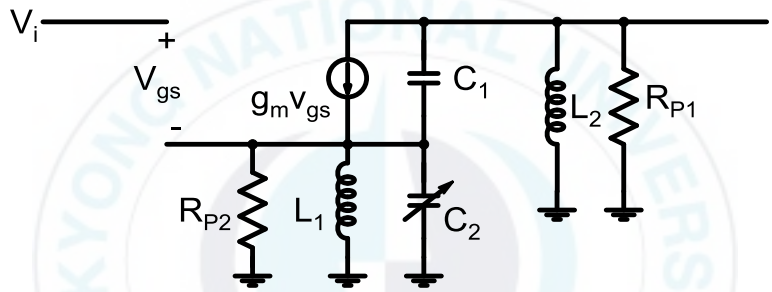


Figure 4.11: Small signal half-circuit model of LC VCO

$$R_{P1} = \frac{\omega^2 L_1^2}{R_{s1}} \tag{4.23}$$

$$R_{P2} = \frac{\omega^2 L_2^2}{R_{s2}} \tag{4.24}$$

where R_{s1} and R_{s2} are the series resistances of L_1 and L_2, respectively.

After cumbersome calculation and proper arrangement of the loop gain unity (V_o/V_i) at ω_0 the result is as expressed in Eq. (4.25) to Eq. (4.26) [57].

$$L_1L_2C_1C_2\omega_0^4 - \left[L_1C_1 + L_2(C_1 + C_2) - \frac{L_1L_2g_m}{R_{p2}}\right]\omega^2 + 1 = 0 \quad (4.25)$$

$$L_1L_2(R_{P1}C_1 + R_{P2}C_1 + R_{P2}C_2) - g_mL_1L_2R_{P1}R_{P2}C_2]\omega_0^3 - [g_mR_{P1}R_{P2}(L_2 - L_1) + L_1R_{P2} + L_2R_{P1}] = 0 \quad (4.26)$$

The oscillation frequency can be approximated as follows:

$$\omega_0 \approx \sqrt{\frac{1}{L_2C_2} + \frac{C_1+C_2}{L_1C_1C_2}} \quad (4.27)$$

In special case when L_1=L_2=L_P and R_{P1}=R_{P2}=R_P, the oscillation frequency in simplified form is as given Eq. (4.278).

$$\omega_0 \approx \sqrt{\frac{1}{L_P}\left(\frac{1}{C_1} + \frac{2}{C_2}\right)} \quad (4.28)$$

$$g_mR_P = 1 + \frac{4(C_1/C_2)^2}{1+2(C_1/C_2)} \quad (4.29)$$

It is obvious from (4.28) that a small variation in C_2 leads to large variation in oscillation frequency. In other words, since C_2 has a large coefficient in the nominator, it has more effect on the ω_0 than C_1 does. Thus, the capacitor C_2 is realized by varactor resulting a wide frequency tuning

range in the proposed current-reuse VCO. Meanwhile, the capacitor C_1 should be very large to have a reasonable tuning frequency at the RF frequency of 24GHz. However according to Eq. (4.29), the C_1/C_2 ratio determines the required transconductance for sustainable oscillation. In other words, the higher C_1/C_2 ratio is, the higher transconductance will be. As a result, there is a sever tradeoff among the power consumption and oscillation frequency range of the VCO by tuning C_1/C_2 ratio. Furthermore, the effect of intrinsic parallel resistances in n/pMOS transistors will be reduced by utilizing the parallel-connected C_1 and C_2 network. This network adjusts the output port load impedance of VCO for improving its performance such as phase noise. As it depicted in Figure 4.12, different values of C_1/C_2 ratio are corresponding to certain phase noises. Thus, by finding the optimized value for capacitor ratio, a subtle tradeoff among different features such as power consumption, amplitude imbalance ratio (the ratio of differential output waveforms: V_{out+}/V_{out-}), and phase noise can be considered. As can be seen in Figure 4.12, when the capacitor ratio is in the interval of [1.37 1.73], the phase noise has the minimum level. However in this interval the differential outputs are not symmetry and the amplitude imbalance ratio gets worse. In addition, as the capacitor ratio is low, the power consumption will be low.

Thus, by considering the above-mentioned tradeoffs, the optimum point is located in the interval of [1.19 1.25].

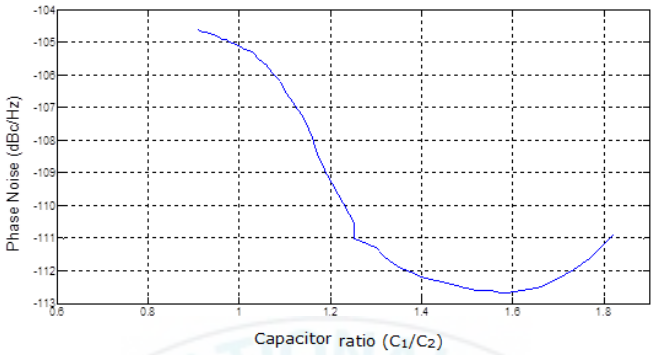


Figure 4.12: Simulated phase noise versus capacitor ratio at 1 MHz offset frequency

4.8.2 Analysis of Output Voltage Swing

In the proposed current-reuse LC VCO, a capacitive-feedback technique including capacitances C_1 and C_2 is utilized to enhance the phase noise and to widen the oscillation frequency tuning. As shown in Figure 4.13, the source terminal of nMOS swings below than ground and drain terminal of pMOS swings above the supply voltage, due to the in-phase relationship which causes by capacitive-feedback technique and inductors. In other words, due to the charging/discharging among inductors and capacitors, the

drain/source voltages of p/nMOS swing above and below than the supply voltage and ground, respectively. To further investigate the oscillation amplitude of the proposed VCO, detailed analysis is provided here.

As explained in the previous section, the losses in the LC tank represent by R_{Pi} (i=1 and 2). In the steady state region, the output voltages are approximated by $V_{on}=V_{dd}-Acos(\varphi)$ and $V_{op}=V_{dd}+Acos(\varphi)$. Here A is the maximum amplitude of VCO and φ is the phase given by $\varphi=\omega_0 t$. The oscillation frequency is given in (4.26). When voltage gain of nMOS reaches its peak value, the maximum drain current ($I_n(t)$) flows. In pMOS case, the maximum drain current happens when its gate voltage reaches its peak. In other words, when $V_{g,n}= V_{dd}+A$ and $V_{g,p}= V_{dd}-A$, maximum drain currents will occur, respectively. As shown in Figure 4.14, I_0 is the maximum amplitude for the drain current in the verge of V-limited and I-limited regions and it is given in Eq. (4.30).

$$I_0 \cong \mu_n C_{0x} \frac{W_n}{L} \left[\left(V_{dd} + \mathrm{A} + \mathrm{nA} - V_{t,n}\right)(V_{dd} - \mathrm{A} + \mathrm{nA}) - \frac{1}{2}(V_{dd} - \mathrm{A} + \mathrm{nA})^2\right. \tag{4.30}$$

where V_t is threshold voltage of MOS transistors, and $n=C_1/(C_1+C_2)$.

The fundamental voltage amplitude of the both positive and negative output ports are expressed in Eq. (4.31) [58].

$$\mathrm{A} \approx \frac{2}{\pi} I_0 R_o \tag{4.31}$$

where R_o is the output load of the VCO. After simplification, the output VCO is given as Eq. (4.32).

$$\mathrm{A} \approx \left(1 + \frac{C_1}{C_2}\right) V_{dd} \tag{4.32}$$

It is obvious from Eq. (4.32) that the output amplitude of proposed current-reuse VCO is a function of C_1/C_2 ratio. As can be seen from Figure 4.15, by apply the capacitive-feedback technique the VCO output swing is larger than the V_{dd}.

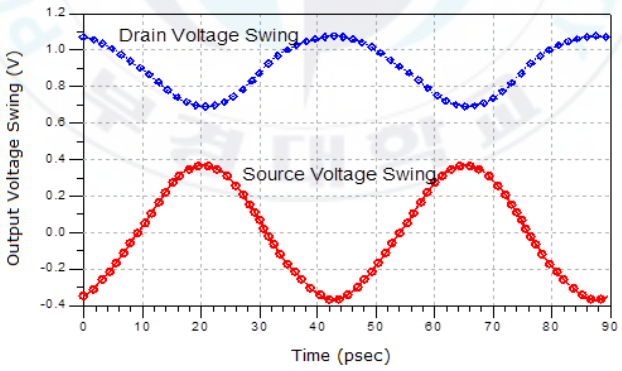


Figure 4.13: nMOS source terminal waveform and pMOS drain terminal waveform

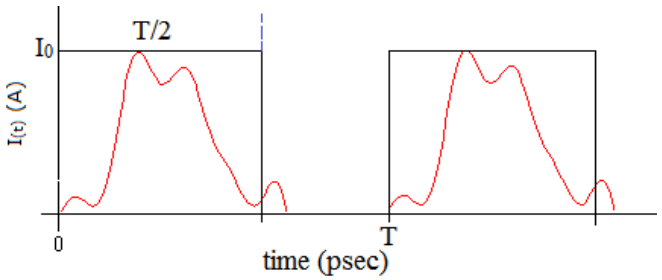


Figure 4. 14: Drain current waveform of M_1

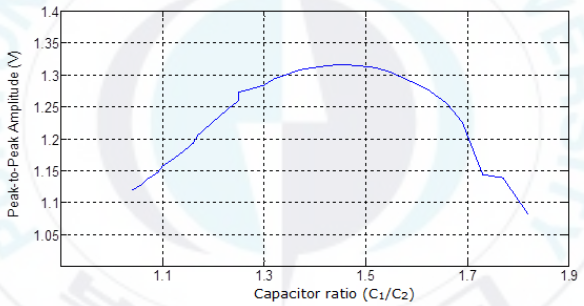


Figure 4.15: Simulated peak-to-peak amplitude at the VCO output

4.8.3 Frequency-Dependent Negative Resistance

The traditional cross-coupled LC VCO [59] compensates the losses of the inductors and capacitors by producing negative resistance (NR). The NR can be generated by utilizing active devices such as MOS and BJT in the VCO core. In the traditional current-reuse technique, there is no negative resistance to compensate the losses to LC tank. Once Hsu et al. [46] proposed negative resistance in the traditional current-reuse to enhance the power consumption under low supply voltage. The idea in [60] was implemented by employing cross-coupled configuration to generate negative resistance. However the power dissipation in the proposed technique got improved, but negative resistance works only at a certain designed frequency and it is no longer valid in the vicinity of oscillation frequency.

In this study, we propose a negative resistance technique that is frequency dependent and can adopt itself to the new frequency automatically. Figure 4.16(a) is a capacitively source-degenerated circuit.

As depicted in Figure 4.16(b), the equivalent input impedance from gate terminal is a negative resistor with a value of $g_m/(C_sC_{gs}\omega^2)$ in series with two series capacitors C_{gs} and C_s [61]. Since resistance loss of on-chip inductors

increases with frequency, the shunt conductance of the proposed negative resistor behaves analogously with respect to frequency. Therefore, this configuration is highly favorable because the loss of on-chip inductors over a wide frequency band can be compensated. Since C_s blocks the dc current, it is necessary to parallel a resistor to this capacitor to provide the dc path required for biasing the common-source transistors. The value of the biasing resistor must be several times larger than the impedance of C_s and small enough to provide the dc current needed for producing the required g_m to compensating the loss of LC tank at those frequencies in which the negative circuits effectively compensate for the loss of on-chip inductors. The capacitively source-degenerated negative resistance is self-biased by thanks to the point A (see Figure 4.10) which functions as virtual ground for current-reuse circuit. As shown in Figure 4.10, the drain terminal, of nMOS is connected to the pMOS gate terminal and pMOS drain terminal is connected to the nMOS gate one. Thus, it is clear in this configuration that two gate terminals have enough voltage to bias the negative resistance without any extra and off-chip bias circuit. As a result, this negative resistance configuration improves VCO phase noise under low power consumption and low supply voltage.

Figure 4.17 illustrates the effect of negative resistor on the phase noise of the current-reuse VCO. As shown in Figure 4.17, the phase noise is enhanced by 2dBc/Hz in comparison with traditional current-reuse LC VCO. Since there is no inductor in designing circuit of capacitively source-degenerated negative resistance, it occupies small area on the layout and die microphotograph.

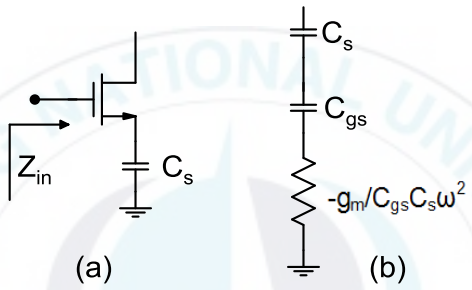


Figure 4.16: (a) Capacitively source-degenerated negative resistance and (b) equivalent input impedance

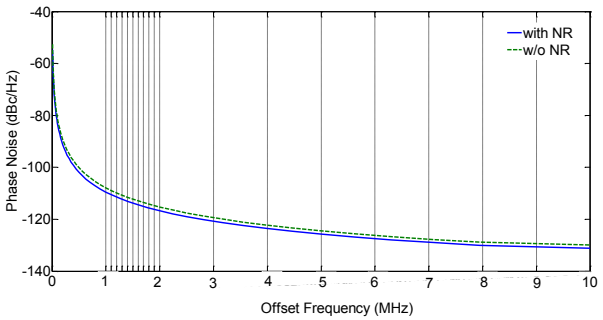


Figure 4.17: Effect of negative resistance on the phase noise of the current-reuse VCO

4.8.4 Phase Noise Analysis

The noise sources of the proposed VCO are depicted in Figure 4.18. In the proposed current-reuse LC VCO, the n/pMOS transistors are biased in the moderate inversion (*MI*) region.

Therefore, with accordance to dc bias point the thermal noise is no longer dominated in the drain noise [25]. To calculate the VCO phase noise, the power densities of noise sources are required. The power density formula of drain current is given by FIGUEW 4.33[61].

$$\overline{i_n^2}\Big/_{\Delta f} = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{gs} - V_t) \tag{4.33}$$

where T is the absolute temperature in Kelvin, γ is a technology-dependent parameter and has a value of around 2/3 for long-channel devices in saturation region (in short channel devices γ is larger and its value is between 2 and 3) [62], Δf is the noise bandwidth in Hz, V_{gs} is the gate-source voltage, V_t is the threshold voltage, C_{ox} is the oxide capacitance per unit area, and μ is the mobility of the carriers in the channel.

In the moderate inversion region dc bias point is close to the threshold voltage. Thus, due to the fact that overdrive voltage $(V_{gs}\text{-}V_t)$ is very small, the drain noise the main contribution of oscillator phase noise will be suppressed. Additionally, the other noise contributor is the effective series resistances of the on-chip inductors result ohmic losses in the substrate and metal, and it is given as Eq. (4.34) [63].

$$\overline{i_{rs}^2}\Big/_{\Delta f} = 4KT\frac{r_s C}{L} = \frac{4kT}{R_p} \tag{4.34}$$

where at the oscillation frequency the parallel resistance is $R_p \approx Q^2 r_s = (L\omega_0)^2/_{r_s}$.

Two capacitively source-degenerated negative resistances are employed in parallel with inductors to eliminate/reduce the effect of series resistance

noise contributor. Therefore, the proposed negative resistance not only results in removing the inductor series resistance, but also suppresses the phase noise leads reducing the total phase noise of the proposed current-reuse LC VCO. Furthermore, capacitive-feedback technique is employed to significantly enhance the output swing resulting an improvement in phase noise.

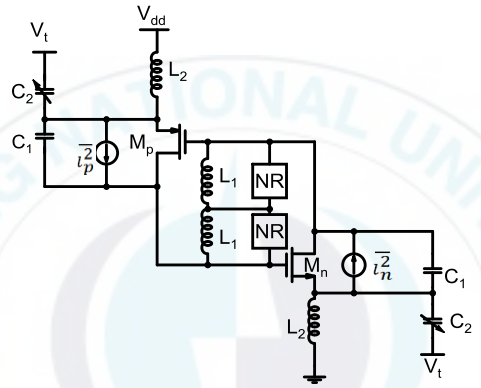


Figure 4.18: Current-reuse LC VCO with source noises

4.9 Results and Discussions

The whole schematic of the proposed current-reuse LC VCO is already illustrated in Figure 4.10 and it consists of n/pMOS transistors in cascode current-reuse configuration to simultaneously boost transconductance and to

save current which leads lowering power consumption. Two buffers in complementary push-pull configuration with feedback resistor (R_f) are utilized to convert the outputs of the VCO to *50*Ω for measuring results. The feedback resistor helps removing bias circuit of the n/pMOS transistors in buffer stage which results in reducing phase noise of the designed VCO. The layout of the proposed VCO is shown in Figure 4.19.

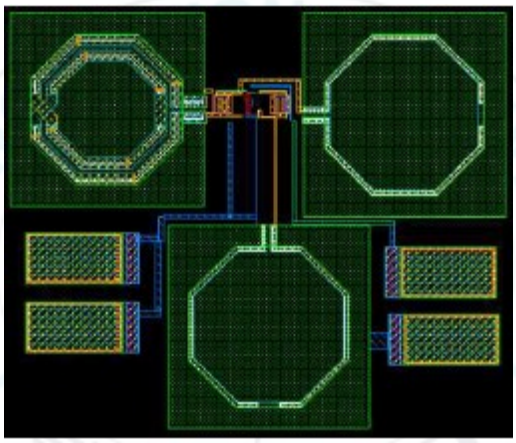


Figure 4.19: The proposed current-reuse LC VCO layout

When circuit is biased at the supply voltage of 0.9 V, the VCO core consumes 411.8μW. A total power of 78.2μW is dissipated by two buffers which operate at the same supply voltage of *0.9 V*. This low power consumption is achieved due to the low supply voltage and cascode current-

reuse structure. The simulated oscillation frequency versus tuning voltage is illustrated in Figure 4.20. The oscillation range from 22.3GHz to 24.3GHz proves that the selection of capacitor C_2 in capacitive-feedback technique as varactor gives an extensively wide tuning range. I-MOS type varactors are used in the VCO circuit design.

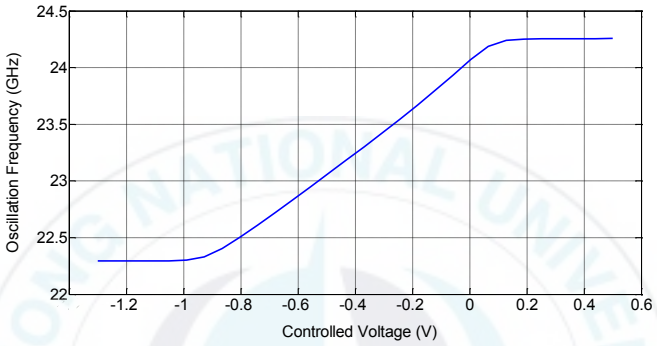


Figure 4.20: Simulated result of the tuning range of the current-reuse LC VCO

The differential output signals are shown in Figure 4.21 with two waveforms of approximately symmetry using current-reuse circuit structure and negative resistance technique.

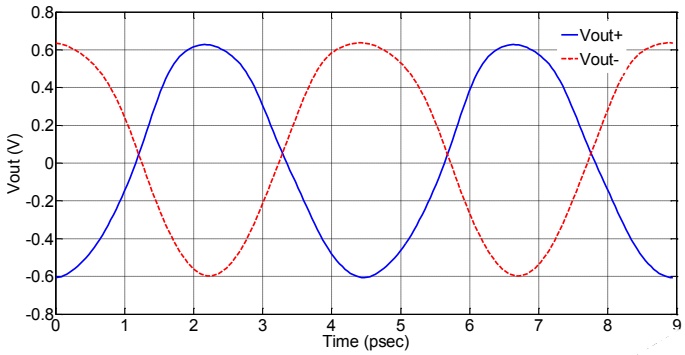


Figure 4.21: Output waveforms of VCO at V_{dd}=*0.9 V* and V_t=*-0.9 V*

Figure 4.22 shows the simulated imbalance ratio of proposed circuit with and without negative resistance over the entire frequency tuning range. As can be seen in Figure 4.21, the amplitude imbalance ratio of the VCO with/without negative resistance at 24GHz and is less than 1and 1.9% and 3.4%, respectively. The proposed negative resistance technique improves the symmetry of the output waveforms which leads to reduce the phase noise.

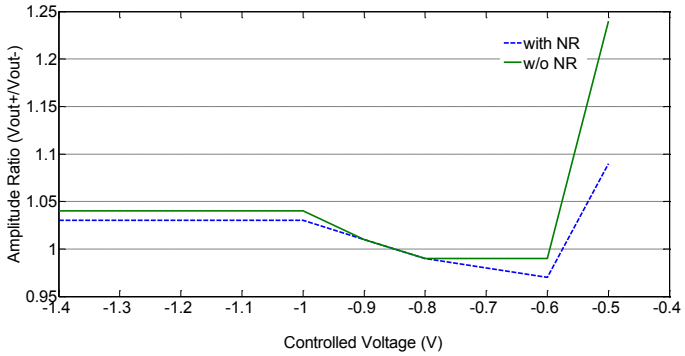


Figure 4.22: Amplitude imbalance ratio of the VCO for controlled voltage (V_t)

The simulated phase noise is -110dBc/Hz at 1MHz as depicted in Figure 4.23.

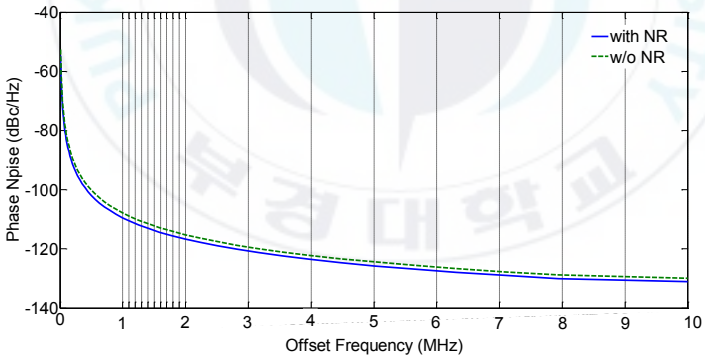


Figure 4.23: Phase noise characteristic of the proposed current-reuse LC VCO

For the sake of comparison with the previous published works, the figure of merits (FOM_T) is defined as Eq. (4.35)[51].

$$FOM^T = \mathcal{L}(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\cdot\frac{F_T}{10}\right) + 10\log\left(\frac{P}{1mW}\right) \quad (4.35)$$

where $\mathcal{L}$ (Δω) is phase noise, and F_T is tuning range percent.

In the end, the performance summary of the proposed LC VCO as compared with other recently published works listed in Table 4.1.

Table 4.1 Comparison of the simulation results of the proposed LC VCO and recently published works

Ref.	**[64]**	**[65]**	**[66]**	**[67]**	**This work**
Tech. (μm)	0.12	0.11	0.18	0.13	**0.13**
Freq. (GHz)	44	24	24	24	**24**
Phase Noise (dBc/Hz)@1MHz	-101	-102	-119	-113	**-110**
Power(mW)	7.5	9	7.2	3	**0.49**
FoM (dBc/Hz)	-184.8	-176.75	-178	-196	**-199.3**

4.10 Summary

An ultra-low power and low phase noise LC VCO in cascode current-reuse configuration has been proposed. A capacitive-feedback technique is utilized to enhance output power and to reduce phase noise. The I-MOS varactors in this technique are placed in parallel with source terminals of n/pMOS which result in a wide tuning oscillation range. Two capacitively source-degenerated negative resistors are employed to eliminate the losses of the on-chip inductors which result in decreasing phase noise of the VCO. The overall circuit including core VCO and two buffers are biased at low supply voltage of 0.9V, and it consumes only 490μW. The phase noise is -110 dBc/Hz at 1MHz offset. A very high FOM of -199.3dBc/Hz has been achieved by including tuning range. An enhancement in terms of power consumption, tuning oscillation range, output symmetry and phase noise is achieved, as a good candidate for 24-GHz radar-based applications.

5 An Integrated High Linearity CMOS Frontend Receiver for 24GHz

5.1 Background

Nowadays, road traffic crashes have become a major global concern. To enhance safety, automotive radar devices are now installing on many transport and luxury passenger vehicles. Automotive radars are utilized in advanced cruise control (*ACC*) systems which can provide information for driver, and actuate a motor vehicle's accelerator and/or brakes to control its distance separation behind another vehicle. Radar-based driver assistance systems also have other important functions such as collision warning systems, blind-spot monitoring, lane-change assistance, rear cross-traffic alerts, back-up parking assistance, collision mitigation systems and vulnerable road user detection.

The receiver for the automotive radar system operates in the band of 24 GHz frequency. Direct conversion receiver (*DCR*) is the best candidate among the various receiver architectures due to the low cost and low power issues. However, large dc offset, LO leakage, *1/f* noise, and I/Q mismatch are bottlenecks of DCR receiver. To alleviate these problems, single

intermediate frequency (IF) DCR architecture has been proposed with the advantage of both the super-heterodyne and DCR architectures [68]. In this receiver type, at first, the incoming signal is converted to IF and then again it is converted to baseband frequency. This operation alleviates the specifications of the receiver backend and enables the analog-to-digital conversion at low frequencies [69]. For this operating frequency, there have been literatures to develope the radar receiver [70-72] and many of them were realized in CMOS technology due to its low cost, technology scaling and high inerrability level.

In this chapter, a low-power, high-linearity and fully integrated receiver frontend is designed in 130-nm CMOS technology for 24 GHz automotive radar application. The proposed circuit is based on single IF DCR architecture and thus it is suitable for silicon integration.

5.2 Proposed Frontend Receiver Architecture

The main wireless receiver task is to detect the desired modulated signals. Wireless receivers have to perform several functions such as tuning to the wanted signal carriers, filtering out the undesired signals, and amplifying the desired signal to compensate for power losses occurring during transmission.

However, there are several receiver architectures, and the heterodyne and the direct conversion are the most popular.

Typically, a heterodyne receiver translates the desired input RF signal into one or more preselected intermediate frequencies before modulation [73]. In this architecture, image rejection and IF filters are vital to avoid folding of interfering signals. Because of presence of several bulky and expensive RF/IF filters, the heterodyne architecture is not suitable for monolithic integration. Enforced by the trends to the cost and size of the RF frontend, alternative heterodyne architecture has been proposed. For instance, direct conversion technique converts the RF signals to the IF-zero baseband in the first frequency downconversion. Therefore, the receiver frontend can be realized in low cost and low power architecture due to the unnecessary off-chip IF filters. Despite superior performances of direct conversion architecture, it suffers from the dc offset and LO leakage which leads to complicate the design and implement of individual blocks to relax the specifications of system.

A modified IF receiver architecture is adopted as a compromise between the heterodyne and the direct conversion to have immunity against flicker noise, dc offset, I/Q mismatch and to achieve higher integration. The block

diagram of the proposed receiver frontend is illustrated in Figure 5.1. First, LNA amplifies the incoming RF signal at 24 GHz. Then the amplified signal is down-converted to a low IF of 10 MHz by the first and second mixer stages. That the quadrature LO signals required for the second mixer are generated by dividing the first LO signal by 2.

The unwanted image signal can be attenuated at least 20 dB by exploiting narrow band characteristic which is provided in the input port of LNA. A LO frequency of 16 GHz is applied to the first mixer to generate signals at an IF band of 8 GHz. Furthermore, the finite bandwidth of receiver frontend leads to suppresse of the spurious band of 40GHz generated by the first mixer stage. A divided-by-2 extended true-single-phase-clock (*E-TSPC*) frequency divider is also designed to provide the quadrature LO signals required for the second mixer stage. Therefore, the output signals of the second mixer stage are located at 10 MHz. In order not to use off-chip components such as buffer, balun and filters, an active balun is adopted to perform three tasks as follows: (*i*) convert the differential output of the second mixer to single-ended output for simulation of the frontend performances; (*ii*) match the output ports of the whole circuits to *50*Ω to achieve S_{22} of less than -10 dB; (*iii*) filter out the undesired image and spurious signals.

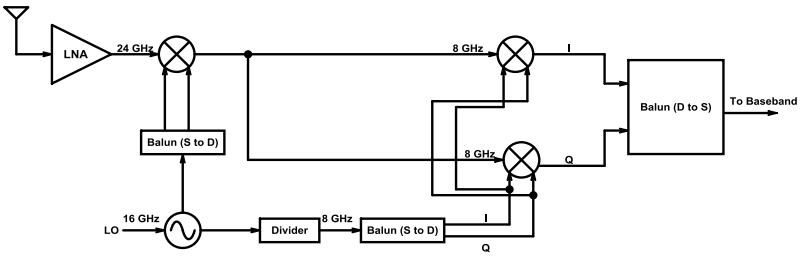


Figure 5.1: Proposed 24 GHz receiver frontend

5.3 Design and Analysis of CMOS Circuit Blocks

5.3.1 LNA

A low noise amplifier (*LNA*) is typically the first active block in the receive path of communication transceivers [74]. The LNA's performance has a direct impact on the linearity, noise figure and power consumption of the entire frontend system [75]. Therefore, tradeoffs for the noise figure, gain and linearity have to be taken into account to find the suitable LNA configuration. Among the RF designers, common source and cascode topologies are the most popular configurations in CMOS technology. At high frequencies, if stability, gain and reverse isolation are taken into consideration, the latter is preferred. However, the degradation of noise figure at high frequencies is the disadvantage of this configuration. To satisfy the LNA tradeoffs, a complementary push-pull (*CPP*) topology [76] is

chosen using pMOS and nMOS transistors which are stacked on top of one another as shown in Figure 5.2. This stacked topology is the most efficient method to maximize the transconductance (g_m) by a fixed dc current, and it enhances the LNA gain as compared to a single common source stage. In CPP topology, the main problem is that at high frequencies the parasitic capacitances cause to degrade the bandwidth and input impedance matching due to the Miller effect. To relax this problem, source inductive degeneration (*SID*) and series-peaking techniques are adopted.

For input impedance matching, the gate inductance (L_g), nMOS source inductance (L_s) and parasitic capacitances of nMOS and pMOS transistors form a multiselection LC ladder to achieve desired input return loss (e.g. S_{11}<*-10 dB*).

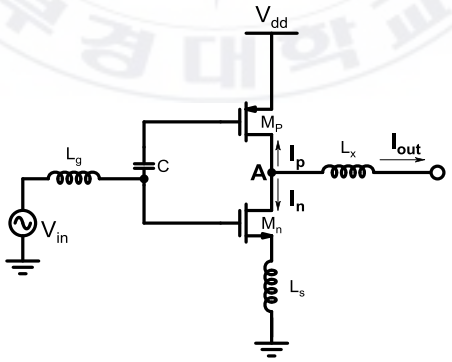


Figure 5.2:Schematic of the proposed complementary push-pull LNA

For further analysis, Figure 5.3 shows the small-signal model of the proposed inverter. Z_{in2} is the impedance seen from point A toward the following stages (i.e. inductor (L_x), mixers, balun), and Z_{in3} is the impedance looking into the coupled source terminal of single balanced mixer. Generally, due to the existence of $C_{gdt} = C_{gdn} + C_{gdp}$, the output impedance effects on the input impedance, and LNA is assumed to be bilateral two-port network. Due to the small value of overlap capacitance C_{gdt}, the Miller effect can be neglected in the practical design. By this assumption, the LNA functions as a unilateral two-port network and the total transconductance of the proposed LNA can be written in Eq. (5.1).

$$g_{m,LNA} = \frac{g_{mn}}{1+j\omega L_S \ g_{mn}} + g_{mp} \tag{5.1}$$

where g_{mn} and g_{mp} are the transconductance of nMOS and pMOS, respectively.

According to Figure 5.3, the voltage gain (A_V) of the LNA is expressed in Eq. (5.2).

$$A_{V,LNA} = g_{m,LNA}[\big((1 + j\omega L_s \ g_{mn})R_{on}\big) \mid |R_{op} \mid |Z_{in2}] \tag{5.2}$$

where R_{on} and R_{op} are the intrinsic output resistances of nMOS and pMOS, respectively.

The input impedance of the proposed LNA can be calculated using the small-signal circuit as given in Eq. (5.3) [2].

$$Z_{in} = j\omega L_g + (j\omega L_s + \frac{1}{j\omega C_{gsn}} + \frac{g_{mn}L_s}{C_{gsn}}) \,||\, \frac{1}{j\omega C_{gsp}} \tag{5.3}$$

where ω is the operation frequency, C_{gsn} and C_{gsp} are the parasitic capacitance of the nMOS and PMOS, respectively.

An inter-stage peaking inductor using L_x, series peaking technique is inserted to isolate the stages from each other. As shown in Figure 5.3, the parasitic capacitance of the inverter topology and following mixer along with L_x form a π section LC filter network at the resonance frequency of 24 GHz to boost gain and bandwidth. By this technique and choosing proper L_x value,

[2] Although, the input impedance of the bilateral LNA (existence of C_{gdl}) is so complicated and time-consuming, but it is provided in Eq. (5.4).

$$Z_{in} = \frac{s^2 C_{gsn} L_s R_{on} + s L_s (g_{mn} R_{on} + 1) + (g_{mn} R_{on} + 1) R_{on}}{s^3 L_s C_{gsn} C_{gdn} R_{on} + s^2 (L_s C_{gsn} + L_s C_{gdn} g_{mn} + L_s C_{gdn} - C_{gsn} C_{gdn} R_{on}) - s(C_{gsn} + C_{gdn} + g_{mn} R_{on} C_{gdn})} \,/\!/\, \frac{s(R_{op} C_{gsp}) + g_{mp} R_{op} + 1}{s^2 C_{gsp} C_{gdp} R_{op} + s[(g_{mp} R_{op} + 1) C_{gdp} + C_{gsp}]} \,/\!/\, Z_{in2} \tag{5.4}$$

the LNA gain roll-off at RF frequency will be compensated, and relatively flat gain can be achieved.

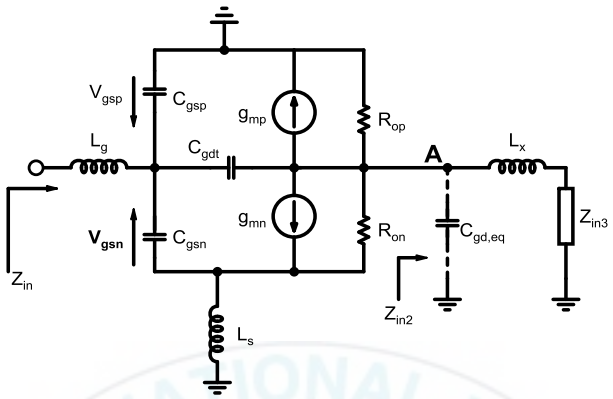


Figure 5.3: Small-signal circuit of the LNA

Due to the possible large interference signals at the input of the LNA, it has to provide high linearity, thus preventing the intermodulation tones created by the interference signal corrupting the carrier signal [77]. Thus, special attention has to be paid to the linearity performance of the LNA in the wireless transceiver design. The proposed CPP topology also addresses simultaneous minimization of the second- and third-order transcondactance of nonlinear coefficients g_{m2} and g_{m3}, respectively. By concurrently incorporating the well-known property of g_{m3} in weak and strong inversion

regions, and the symmetric property of second-order nonlinear coefficient (g_{m2}) around sweet-spot, g_{m3} crosses zero in moderate inversion region [78]. The transfer function of nMOS and pMOS are described in Eqs. (5.5) and (5.6), respectively.

$$i_n = g_{m1n}v_{gsn} + g_{m2n}v_{gsn}^2 + g_{m3n}v_{gsn}^3 + \cdots \quad (5.5)$$

$$i_p = -g_{m1p}v_{gsp} + g_{m2p}v_{gsp}^2 - g_{m3p}v_{gsp}^3 + \cdots \quad (5.6)$$

where g_{m1} is the main transconductance of the MOSFET, g_{m2} is the second-order nonlinear coefficient obtained by the second-order derivative of the dc transfer characteristic, and g_{m3} is the third-order nonlinear coefficient obtained by the third-order derivative of the dc transfer characteristic.

Since v_{gsp} is a function of v_{gsn}, it can be expanded into power series of v_{gsn} expressed in Eq. (5.7).

$$v_{gsp} = c_1v_{gsn} + c_2v_{gsn}^2 + c_3v_{gsn}^3 \quad (5.7)$$

From the bias circuit theory, it is clear that the c_1 has positive value and the c_2 and c_3 values are negligible. As can be seen in Figure 5.2, we have Eq. (5.8).

$$i_{out} = i_n - i_p = (g_{m1n}+g_{m1p})v_{gsn} + (g_{m2n} - g_{m2p})v_{gsn}^2 + (g_{m3n} + g_{m3p})v_{gsn}^3 \quad (5.8)$$

Figure 5.4 shows the simulated drain currents and their derivatives with respect to V_{gs} for nMOS and pMOS transistors operating in the strong inversion region. The third-order nonlinear coefficients of nMOS and pMOS transistors are shown in Figure 5.4(c). As can be seen, gate bias voltages and sizes of the transistors are chosen to align the positive peak of the pMOS transistor with the negative peak of the nMOS resulting in the g_{m3} with almost zero value.

The *IIP3* of a nonlinear device is defined in Eq. (5.9) [76].

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{5.9}$$

By using CPP configuration, and choosing appropriate gate voltages and sizes of transistors, *IIP3* of the LNA can be improved. With a simple analysis, the proposed technique can boost g_{m1} as shown in Figure 5.4(a) and it can reduce g_{m3}. Therefore, CPP technique can highly improve linear performance of the LNA in the operation frequency range.

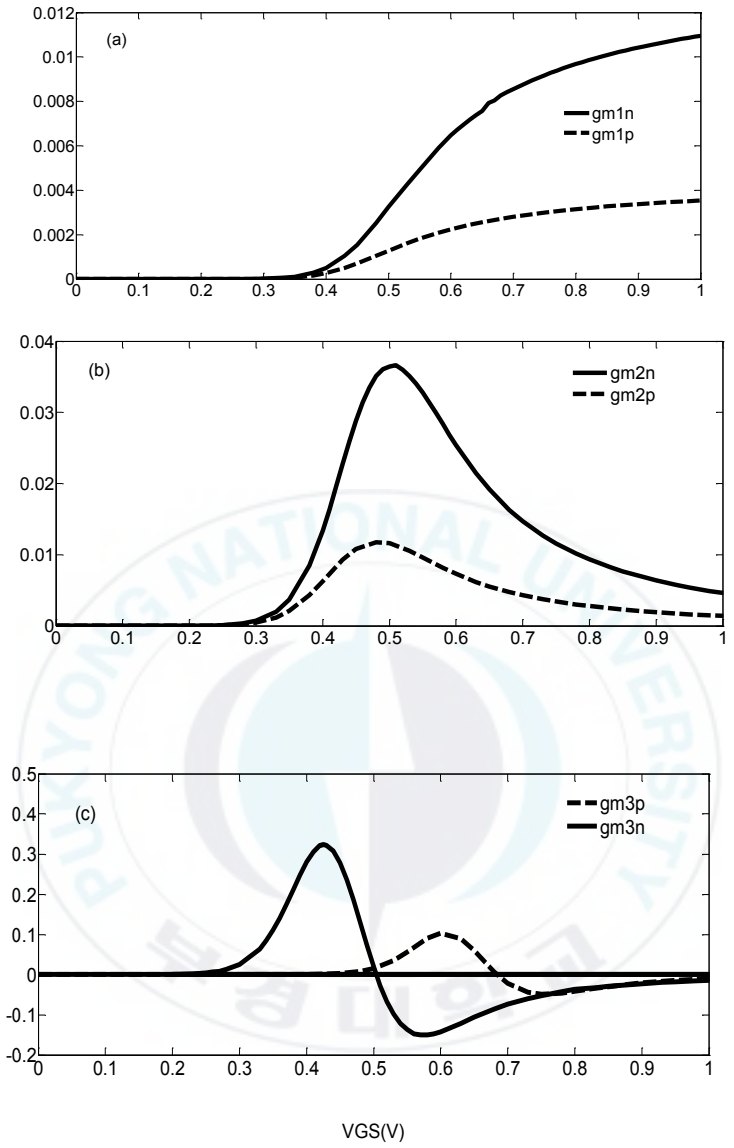


Figure 5.4: (a) Simulated g_{m1n} and $g_{m1p,}$ (b) simulated g_{m2p} and $g_{m2p,}$ (c) simulated g_{m3n} and g_{m3p}

5.3.2 Mixer

The simplified schematic diagram of conventional I/Q mixer is shown in Figure 5.5(a). It is composed of two cascased mixers, and each mixer consists of voltage to current (*V-I*) converter, Gilbert cell and current to voltage (*I-V*) converter. As can be seen, the V-I converting transconductor converts the applied input voltage signal to current which is steered by the first mixer switch. The first mixer converts the high frequency current signal to IF signal. Then the translated signal at the output of the first mixer is reconverted to voltage by the I-V trans-resistor converter. The second V-I converter again converts the IF voltage signal to current for the chopping function. The second Gilbert cell mixer converts IF current signal to baseband one, and ultimately the second I-V converting trans-resistor converts the steered current to voltage at the output port. High power consumption and low linearity are bottlenecks of this traditional architecture. The former comes from cascode structure in the first and second stages, and the latter is due to the existence of I-V and V-I converters. Figure 5.5(b) illustrates the proposed circuit to alleviate drawbacks of the conventional architecture. First, to avoid selection of cascode topology, a folded structure has been chosen. Folded mixers have become popular structure for high

linearity and low-voltage operation. It is possible to avoid stacking transistors with a folded mixer [79]. However, folding the circuit adds additional current branches. By utilizing folded structure, the voltage headroom will be also increased. Furthermore, the first V-I converter is deleted and replaced by a CPP topology which functions as an LNA to increase the linearity and gain.

Second, the first mixer is realized using pMOS transistor. Having pMOS switches in LO stage helps to achieve same overdrive voltage and consequently similar linearity performance with lower power consumption compared to the case using nMOS transistors [80]. Finally, the first and the second I-V converterare realized in resistor to avoid employing inductor which leads to occupy large die area. Moreover, the second V-I converter is removed, and this causes the double balanced mixer connects directly to the first switch mixer.

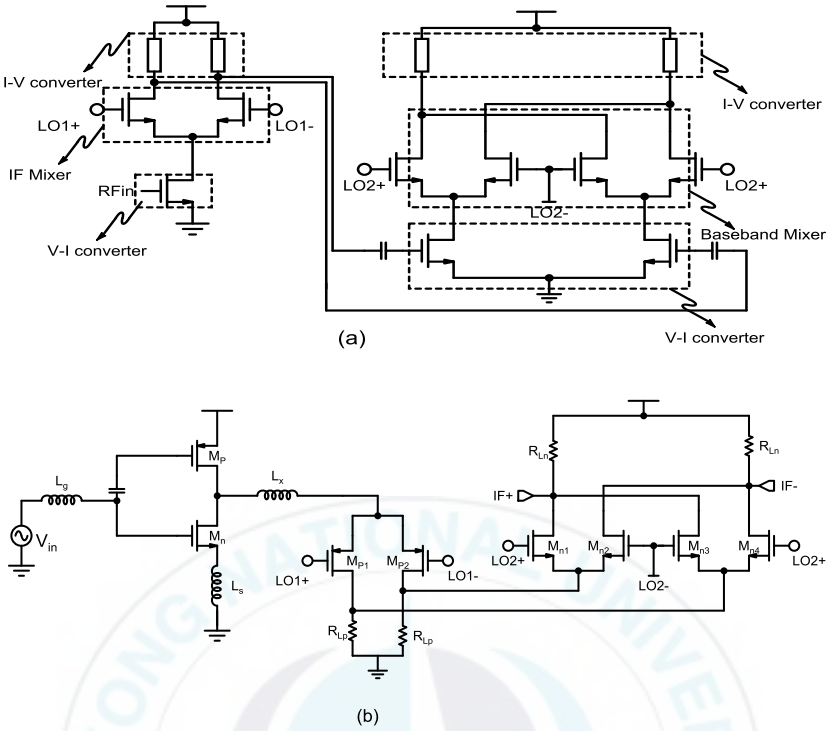


Figure 5.5: (a) Conventional mixer with two stage and (b) proposed mixer using folded architecture

Low power consumption and low voltage operation are two essential requirements for mixers. Low voltage mixers are challengeable because traditional mixers rely on stacking multiple transistors [81]. In addition, circuits designed with MOS transistors biased in subthreshold region operate with lowered voltage headroom, resulting in smaller power supply and

further reduced dc power dissipation [82]. Thus, the proposed mixer switches are biased in subthreshold region to reduce the power consumption. Furthermore, Figure 5.6 clearly depicts that by biasing the switch transistors in weak inversion region, a gain enhancement of 10 dB will be yielded in comparison with biasing in strong inversion region.

There is another benefit to operate the mixer transistors in subthreshold inversion region. With this assumption all switch transistors have constant transconductance in subthreshold inversion, and the noise performance will be significantly improved compared to strong inversion. There are two types of noise in RF frontend. First, flicker noise which is inversely proportional to transistor size, and a weakly inverted transistor will be considerably larger than a strongly inverted transistor. Second, thermal noise will be reduced because the value of the drain thermal noise factor (γ) which is approximately 25% smaller in weak inversion [83]. Meanwhile, in subthreshold region the required LO signal power is expected to be smaller, and it leads to reduce the dc power consumption of LO signal generator.

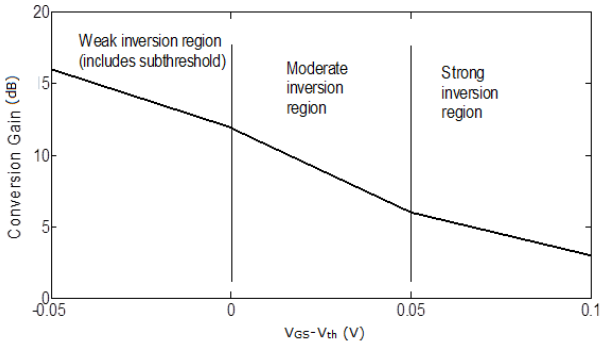


Figure 5.6: Conversion gain versus mixer transistor regions

5.3.3 Frequency Divider

Frequency divider is the most challengeable stage in the receiver frontend and it must be carefully designed to meet the speed specifications and to keep power consumption at a low level, simultaneously. Current-mode-logic (*CML*) latches have been utilized in conventional high speed flip-flop (*FF*)-based divider which has a large capacitance load. This not only increases the power consumption of the whole circuit, but also confines the operating frequency and current-drive ability. To reduce power consumption, the true-single-phase-clock (*TSPC*) divider was emerged. However, its operation was confined to the low frequency range. Ultimately, extended TSPC (*E-TSPC*) divider is designed for high speed and low power consumption. E-TSPC divider cancels the transistor with stacked structure so that all transistors are

free from the body effect. Thus, they are more suitable for high operating frequency applications with low power supply [84].

Figure 5.7 displays the proposed E-TSPC which is composed of three pMOSs and three nMOSs. Their aspect ratios are obtained by employing the classical domino logic scaling [85]. The sizes of the transistors are chosen in a way to achieve good matching at the expense of operating frequency and dynamic power consumption.

The input and output results of the frequency divider are shown in Figure 5.8. As can be seen, the divider not only divides the input frequency by two precisely, but also amplifies the input signal at the output port (V_{out}). Therefore, the I/Q mixers operate in a LO power which is attractive for highly integrated ICs with low power consumption.

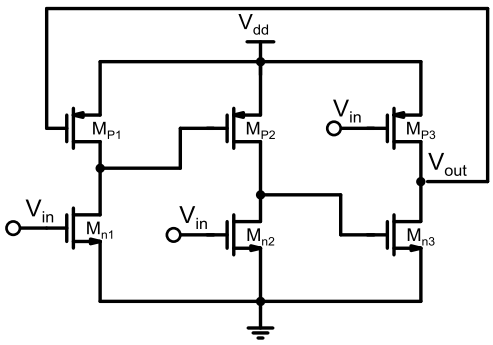


Figure 5.7: Divided-by-2 E-TSPC frequency divider

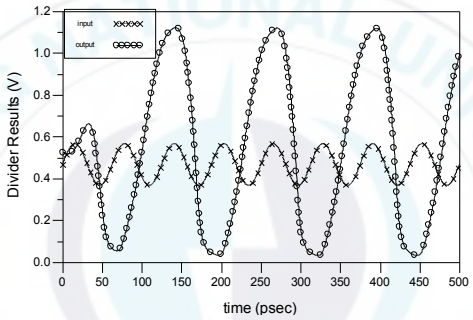


Figure 5.8: Input and output waveforms of the divided-by-2 frequency divider with an input frequency of 16 GHz

5.3.4 Balun

One of the most common problems in receiver frontend designs is that the LO source is single-ended and should be connected to the differential

input mixer. One solution is to use passive balun implemented on board which is much bulkier than a silicon micro-strip line circuit, and the other solution is to utilize micro-strip lines for designing balance to unbalanced converter. To alleviate the foregoing drawbacks, an active narrow band balun which is shown in Figure 5.9 is developed to convert the single-ended input to differential structure with a high gain precision for the entire band of 23.5 to 24.6 GHz. The proposed active balun consists of nMOS and pMOS pair configuring in inverter type. As shown in this configuration, nMOS stacked on top of pMOS behaves as common source and common gate, respectively. This topology reuses the dc current and leads to reduce power consumption. To reduce the deteriorative output parasitic capacitance influence of balun and parasitic capacitance of following mixers, inductors L_n and L_p are placed. These inductors with intrinsic capacitors of transistors form LC filter, resonant at 8GHz frequency to increase the conversion gain and boost the voltage headroom by reducing the voltage drop across the transistor loads.

Figure 5.10 shows the simulated gain difference (*GD*) as well as phase difference (*PD*) versus frequency. The proposed balun provides gain and phase imbalance within only 0.5 dB and 3^{o} over the frequency band of 23.5 to 24.5 GHz, respectively.

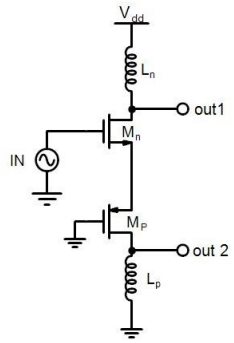


Figure 5.9: Circuit schematic of single- to differential-ended balun

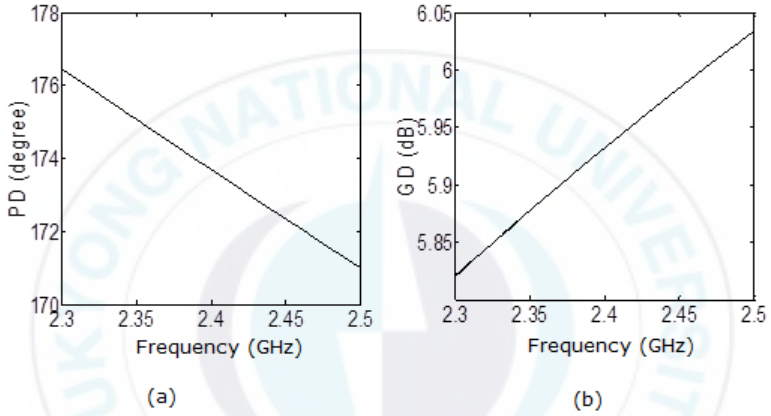


Figure 5.10: (a) Phase difference (*PD*) and (b) gain difference (*GD*) between the output ports of S-D balun

The S-D balun has been directly utilized after the local oscillation generator for stimulation of the I-mixers as well as utilized after frequency

divider to convert single-ended balun to double structure for the Q-mixers in the proposed receiver frontend architecture.

Finally, to enhance the integrity of the whole circuit, an active balun is designed and used at the output ports of mixer stage. This balun converts the differential-ended mixer outputs to single-ended output (*D-S*) which can be connected to next stage without off-chip device. Figure 5.11 illustrates the push-pull balun composed of both common-source and common-drain configurations with advantages of low power consumption and good isolation. Resistor R_d is inserted to provide *50Ω* to IF output impedance matching for down-conversion mixer. The signal gain of D-S balun is the sum of the two signal path gains [86]. Therefore, the D-S balun functions as a buffer and differential- ended single-ended converter, simultaneously.

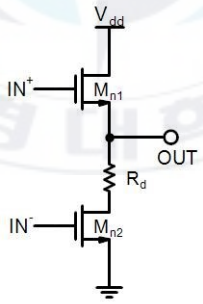


Figure 5.11: Circuit schematic of the output differential-ended to single-ended balun

5.4 Results and Discussions

The Proposed 24 GHz receiver frontend is designed and simulated in 180-nm TSMC CMOS process. The receiver frontend parameters are listed in Tables 5.1 and Table 5.2.

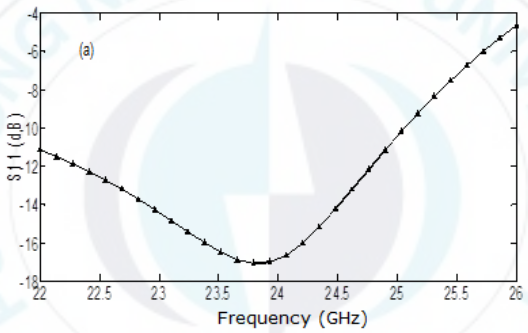
Table 5.1 Circuit parameters of LNA and mixers

LNA	
M_n	72µm/0.18µm
M_p	24µm/0.18µm
L_g	0.3nH
L_s	0.25nH
L_x	0.85nH
IF Mixer	
M_{P1}, M_{P2}	20µm /0.18µm
R_{LP}	5kΩ
Baseband Mixer	
M_{n1}, M_{n2}, M_{n3}, M_{n4}	22µm/0.18µm
R_{Ln}	0.3kΩ

Table 5.2 Circuit parameters of divider and baluns

Divider	
M_{n1}	0.3μm/0.18μm
M_{n2} , M_{n3}	3 μm/0.18μm
M_{P1}	1.54μm/0.18μm
M_{P2}	2 μm/0.18μm
M_{P3}	3.54μm/0.18μm
S-D Balun	
M_n	9μm/0.18μm
M_p	18μm/0.18μm
L_n	7nH
L_p	8nH
D-S Balun	
M_{n1}	20μm/0.18μm
M_{n2}	7μm/0.18μm
R_d	0.6kΩ

The simulation is done at *1.5 V* with dc current of 4.33 mA. The input and output reflection coefficients, S_{11} and S_{22}, are illustrated in Figure 5.12 exhibiting a value better than -10 dB within the entire frequency range. The RF input port and the IF output port are well matched at their respective frequencies. For input impedance matching, the gate inductance (L_g), nMOS source inductance (L_s), and parasitic capacitance of nMOS and pMOS transistors form a multiselection LC ladder to achieve desired input return loss (e.g. S_{11}<*-10 dB*).



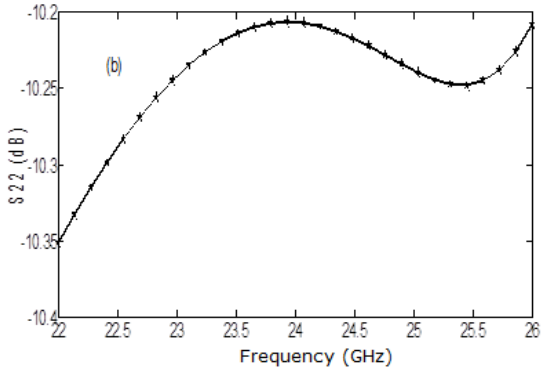


Figure 5.12: Reflection coefficient of the proposed frontend versus frequency: (a) Input return loss (S_{11}), (b) Output return loss (S_{22})

The second stage of the proposed frontend is mixer that realized in I/Q structure to convert RF frequency to baseband frequency. First, high frequency is translated into IF frequency by utilizing single balanced mixer type. This single balanced switch adopts pMOS transistors to increase the linearity and voltage headroom, and hence to reduce power consumption. Furthermore, this switch mixer is realized in folded cascode topology and does not need independent biasing circuit. A double balanced Gilbert cell mixer is designed to translate IF frequency into baseband frequency. The whole transistors in mixer stage (second stage of the frontend receiver) are

biased in subthreshold region to reduce the power consumption. Since transistors in mixer stage consume low power from the supply voltage, the voltage drop across the mixer loads are small and large resistors can be used in the output port of two mixers. Therefore, these large resistors lead to increase conversion gain of the receiver.

A single-ended to differential-ended (*S-D*) balun is exploited at the output port of LO signal generator for the sake of stimulating mixer transistors. An active on-chip differential-ended to single-ended (*D-S*) balun is also adopted to simulate the conversion gain of the whole circuit shown in Figure 5.13. The simulation exhibits that maximum power gain of 19.6-dB appears for a 24 GHz. The D-S balun also functions as a buffer which provides 50-Ω impedance for the output, and the matching result is shown in Figure 5.12(b) (i.e. S_{22}<*-10 dB*). Both of the active baluns adopt cascode configuration to reduce the power consumption. Although S-D balun exploits two inductors in the output ports, it provides approximately identical and out-of-phase signals which are suitable for proposed receiver. Additionally, these active and on-chip baluns increase the integrity level of the receiver frontend.

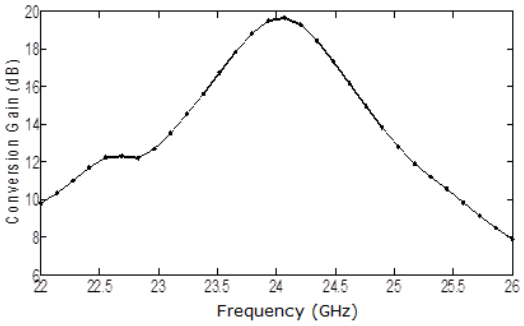


Figure 5.13: Conversion gain versus frequency with 24-GHz LO signal

Figure 5.14 depicts that the proposed frontend features a NF of 11.2 to12.1 dB in 3-dB bandwidth.

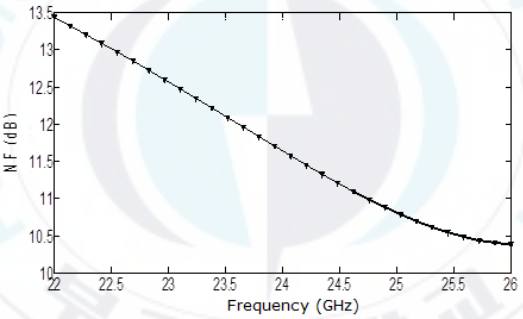


Figure 5.14: Total noise figure of the proposed frontend versus frequency

With the nature of cascading stages, the linearity of the receiver frontend mainly depends on the LNA and mixer. In this study, the complementary push-pull topology is adopted in the LNA stage for the improvement of gain

compression and third-order intercept point (*IIP3*). Alternatively, the desirable circuit linearity is achieved by optimizing the device size and bias condition of this particular design. The IIP3 versus input RF power is illustrated in Figure 5.15. The simulation illustrates good IIP3 of 3 dBm for the proposed frontend.

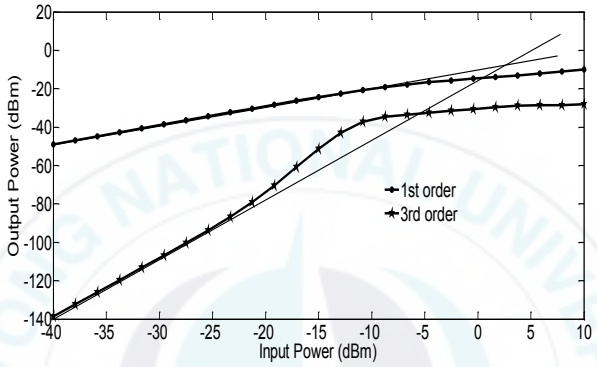


Figure 5.15: IIP3 of the proposed frontend versus RF power

The performance summary of the proposed receiver frontend and comparison with other high-linear published works are shown in Table 5.3. As can be seen, the proposed receiver frontend performs very well in linearity and power consumption.

Table 5.3 Comparison of the results of the proposed receiver frontend and recently published works

Ref.	**[70]**	**[71]**	**[81]**	**[87]**	This work
Tech (nm)	180	180	130	130	130
Freq (GHz)	24	24	24	24	24
Conversion Gain (dB)	28.4	27.5	30	24	19.6
NF (dB)	6	7.7	6	5.1	11.6
Power(mW)	54	43	540	3.78	6.5
IIP3 (dBm)	-13	-23[a]	-35[@]	-13	3

[@] P_{1dB}

5.5 Summary

A single-ended receiver frontend has been presented for 24-GHz automotive radar. By integrating the two-stage LNA and downconversion mixers, the frontend has been designed in 130-nm CMOS technology. The LNA stage was adopted complemenptary push-pull (*CPP*) topology to boost the gain and the linearity of whole circuit. Meanwhile, the LNA was realized in folded configuration to reduce power supply and to increase voltage headroom. The frontend was realized in IF-DCR architecture to increase integration level and to alleviate the DCR problems. Two active baluns were also designed to increase the integrity of the frontend. Furthermore, the switch transistors were biased in subthreshold region to reduce the power consumption. The proposed receiver frontend showed high conversion gain of 19.6dB, NF of 11.2 to 12.1dB, good IIP3 of 3dBm and low power dissipation of 6.5mW.

6 Conclusion

6.1 Conclusions

Automotive collision avoidance radar devices are now installing on many transport and luxury passenger vehicles to enhance safety. These radar-based devices are implemented in a receiver frontend to reach the predefined goals. Recently, different blocks of transceivers should place on single chip to improve the integrity level as much as possible. Furthermore, most of wireless portable devices need long battery-life which realizes with designing low power blocks in the receiver chain such as low noise amplifier (*LNA*), mixer and voltage-controlled oscillator (*VCO*). This dissertation addressed low power, low noise and high linearity LNA, mixer and VCO, which are critical stages in the receiver chain. This dissertation also aims to increase the integrity level of frontend with designing all of the building blocks on the single chip.

The LNA is realized in the complementary push-pull (*CPP*) configuration to increase the transconductance (g_m) and gain. This topology also utilized to save power consumption. In the CPP configuration, the pMOS transistor is placed on top of nMOS one. The nMOS transistor

consumes the current of pMOS transistor which leads to save current and power consumption. Meanwhile, the LNA was realized in folded configuration to reduce power supply and to increase voltage headroom. The CPP topology improves the linearity by eliminating/reducing the second-order transconductance (g_{m2}) and third-order transconductance (g_{m3}), simultaneously. Due to the input and source inductors, good input matching (S_{11}) is achieved.

Furthermore, the two-stage LNA for UMTS and 4G LTE applications was proposed to achieve high linearity by using MBDS technique. This technique was formed by two parallel transistors to improve the linearity performance. We achieved high linearity using the main transistor of nMOS biased in the strong inversion region and the auxiliary bipolar transistor biased in active region. To linearize MOS devices in CMOS technology, the usable possibility of BJT was also explored.

A folded cascode mixer is proposed to reduce the power consumption. In the proposed mixer, the G_m-stage has been removed to reduce the supply voltage and to increase the voltage headroom. The transistors in the switching stage are biased in the subthreshold to reduce the power consumption. In the folded cascode structure, the LNA is placed instead of

current source in G_m-stage to increase the conversion gain and hence reduce the noise figure. Finally, by utilizing the proposed mixer, excellent port to port isolations have been achieved.

An ultra-low power and low phase noise in cascode current-reuse configuration has been proposed. A capacitive-feedback technique is utilized to enhance output power and phase noise. The I-MOS varactors in capacitive-feedback technique are placed in parallel with source terminals of n/pMOS which results in a wide tuning oscillation range. Two capacitively source-degenerated negative resistors are employed to eliminate the losses of the on-chip inductance which result in improving phase noise of the VCO. The overall circuit including core VCO and two buffers are biased at low supply voltage to consume low power. An enhancement in terms of power consumption, tuning oscillation range, and phase noise is achieved, as it a good candidate for 24GHz radar-based applications.

The receiver for the automotive radar system operates in the band of 24-GHz frequency. Direct conversion receiver (*DCR*) is the best candidate among the various receiver architectures due to the low cost and low power issues. However, large dc offset, LO leakage, *1/f* noise, and I/Q mismatch are bottlenecks of DCR receiver. To alleviate these problems, single

intermediate frequency (*IF*) DCR architecture has been proposed with the advantage of both the super-heterodyne and DCR architectures. In this receiver type, at first, the incoming signal is converted to IF and then again it is converted to baseband frequency. This operation alleviates the specifications of the receiver backend and it enables the analog-to-digital conversion at low frequencies. Two active baluns were also designed to increase the integrity of the frontend. Furthermore, the switch transistors were biased in subthreshold region to reduce the power consumption.

Utilizing a standard 130-nm CMOS process, a RF frontend is designed at 24 GHz for automotive collision avoidance radar application. Single IF direct conversion receiver (DCR) architecture is adopted to achieve high integration level and to alleviate the DCR problem. The proposed frontend is composed of a two-stage LNA and downconversion mixers. To save power consumption, and to enhance gain and linearity, stacked nMOS/pMOS g_m-boosting technique is employed in the design of LNA as the first stage. The switch transistors in the mixing stage are biased in subthreshold region to achieve low power consumption. The single balanced mixer is designed in pMOS transistors and is also realized based on the well-known folded architecture to increase voltage headroom. This frontend circuit features

enhancement in gain, linearity, and power dissipation. The proposed circuit shows a maximum conversion gain of 19.6 dB and noise figure of 11.2-12.1 dB within the entire frequency band. It also showed input and output return losses of less than -10 dB within bandwidth. Furthermore, the port-to-port isolation illustrated excellent characteristic between two ports. This frontend showed the third-order input intercept point (*IIP3*) of 3 dBm for the whole circuit with power dissipation of 6.5 mW from a 1.5 V supply.

6.2 Future Works

The automotive industry's efforts to achieve a goal of zero automotive-related fatalities, along with meeting consumer demand and government legislation, are driving adoption of advanced automotive safety systems. Advanced driver assistance systems (ADAS), radar and camera systems are expected to become government-mandated in the future. Freescale's 77 GHz silicon germanium (SiGe) chipset advances automotive safety by enabling vehicles to sense potential crash situations. This radar solution provides long- and mid-range functionality, allowing automotive systems to monitor the environment around the vehicle to help prevent crashes. Freescale's radar

system is based on multichannel receivers and transmitters that allow high-level integration and complex signal generation and processing.

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LIST PUBLICATIONS

(1) Journals

Paper Title	Date	Journal Title
Low Phase Noise and Low Power CMOS Current-reuse LC VCO	Under review	IEEE Microwave and Wireless Components Letters (**SCI**)
24GHz CMOS Power Amplifier for Automotive Radar	January 2017	International Journal of Control and Automation (**SCOPUS**)
Design of Low-Power 24GHz Voltage-Controlled Oscillator	December 2016	AETA (**SCOPUS**)
An Integrated High Linearity CMOS Receiver Frontend for 24-GHz Radar Application	October 2016	Journal of Semiconductor Technology and Science (**SCIE**)
A 2-GHz 20-dBm Low-Power CMOS LNA with Modified DS Linearization Technique	August 2016	Journal of Semiconductor Technology and Science (**SCIE**)
A Broadband Low Noise Amplifier with Built-In Linearizer In 0.13-μm CMOS Process	June 2015	Microelectronics Journal (**SCIE**)
High-Gain and Low-Power Power Amplifier for 24-GHz Automotive Radars	February 2015	International Journal of Smart Home (**SCOPUS**)

(2) Conferences

Paper Title	Date	Conference Title
Design of Low-Power 24GHz Voltage-Controlled Oscillator	December 2016	The International Conference on Advanced Engineering-Theory and Applications 2016
Design of Digital FIR Filters for Noise Cancellation	October 2016	Proceedings of Conference on Information and Communication Engineering

Low-Power 24-GHz CMOS Low Noise Amplifier	October 2016	Proceedings of Conference on Information and Communication Engineering
A low power 12-bit 1MSps SAR ADC with capacitor array network	October 2016	2016 년도 한국멀티미디어학회 추계학술발표대회 논문집 제 19 권 2 호
An Ultra-Low Power 24GHz CMOS LC VCO	October 2016	2016 년도 한국멀티미디어학회 추계학술발표대회 논문집 제 19 권 2 호
12-bit 1MSps SAR ADC for System-on-Chip	June 2016	대한전자공학회 전자·통신 학술대회
Automotive Radar Frontend Circuit in 0.13μm CMOS	June 2016	대한전자공학회 전자·통신 학술대회
Design of a Low Area 12-bit SAR ADC using MOS Capacitor	June 2016	대한전자공학회 전자·통신 학술대회
Development automobile engine measurement device using a laser and a CCD linear sensor.	June 2016	대한전자공학회 전자·통신 학술대회
FPGA implementation of programmable FIR/IIR filter	June 2016	International Conference on Future Information and Communication Engineering
5.25-GHz BiCMOS Low Noise Amplifier	May 2016	Proceedings of Conference on Information and Communication Engineering
Design of Bias Circuit for GHz BiCMOS Low Noise Amplifier	May 2016	Proceedings of Conference on Information and

		Communication Engineering
High Gain 24-GHz CMOS Low Noise Amplifier	May 2016	Proceedings of Conference on Information and Communication Engineering
Development of DPSD(Digital Position Scanning Device) Using Laser and Linear CCD Sensor	December 2015	한국통신학회 학술심포지움 논문집
The Low Area 12-bit SAR ADC using CMOS Process	December 2015	한국통신학회 학술심포지움 논문집
Development of Low-Power CMOS Programmable Gain Amplifier	October 2015	ISAE 2015 International Symposium on Advanced Engineering
The High-Linearity CMOS LNA using Modified DS Linearization Technique	October 2015	ISAE 2015 International Symposium on Advanced Engineering
Fabrication of a Low-Cost Wafer-Level Packaging for RF Devices	October 2015	ISAE 2015 International Symposium on Advanced Engineering
Design of power Amplifier for 24-Applications	October 2015	ISAE 2015 International Symposium on Advanced Engineering
Design of Low-Power Voltage-Controlled Oscillator for 24-GHz Applications	October 2015	Proceedings of Conference on Information and Communication Engineering
Implementation of Vehicle Collision Avoidance Algorithm for Automotive Radar Sensor	October 2015	Proceedings of Conference on Information and Communication Engineering
The Low Area 12-bit SAR ADC	October 2015	Proceedings of Conference on Information and Communication Engineering
77-GHz 저전력 전압제어발진기 설계	October 2015	2015 한국정보기술학회 ICT 논문 경진 대회 논문집
Design of 24-GHz/77-GHz Dual	May 2015	Proceedings of Conference

Band CMOS Low Noise Amplifier		on Information and Communication
Design of 77-GHz CMOS Power Amplifier	May 2015	Proceedings of Conference on Information and Communication Engineering
A Low-Noise and Low-Power LNA and Mixer for 24-GHz Application	December 2014	*The 8th International Conference on Future Generation Communication and Networking*, Advanced Science and Technology Letters
A New CMOS Programmable Gain Amplifier with a DC-offset Cancellation Circuit	December 2014	*The 8th International Conference on Future Generation Communication and Networking*, Advanced Science and Technology Letters
A 12-bit 1MSps SAR ADC using MOS Capacitor	October 2014	*Proceedings of Conference on Information and Communication Engineering*
Design of Low-Power Programmable Gain Amplifier with DC-offset Cancellation	October 2014	*Proceedings of Conference on Information and Communication Engineering*
Design of 77GHz CMOS Low Noise Amplifier with High Gain and Low Noise	October 2014	*Proceedings of Conference on Information and Communication Engineering*
Design of 24GHz CMOS Mixer with High Conversion and Low Power	October 2014	*Proceedings of Conference on Information and Communication Engineering*
A High Linearity Ultra-Wide-Band (UWB) LNA	May 2014	*The Proceedings of the 2014 KIIT Summer Conference*
Design of a Low-Power 12-bit 1MSps SAR ADC	May 2014	*Proceedings of Conference on Information and Communication*

		Engineering
Power Amplifier for Short Range Radar Application of Automotive Collision Avoidance	May 2014	*Proceedings of Conference on Information and Communication Engineering*
Design of 77-GHz CMOS Mixer for Long Range Radar Application of Automotive Collision Avoidance	May 2014	*Proceedings of Conference on Information and Communication Engineering*
Design of Vehicle Collision Avoidance Algorithm for 24GHz/77GHz Automotive Radar Sensor	May 2014	*Proceedings of Conference on Information and Communication Engineering*