Thesis for the Degree of Master of Engineering

24GHz Frequency Synthesizer for Automotive Radar Applications

차량 레이더용 24GH 주파수 합성기

By

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Department of Information and Communications Engineering

The Graduation School

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Contents

Figure List

Table List

24GHz Frequency Synthesizer for Automotive Radar Applications

Abstract

In the recent years the needs for high integration and low cost wireless transceiver modules have been raised and the power consumption is a great consternationfor radio frequency integrated circuit (RFIC) engineers. Rigorous attempts havebeen made to provide RF systems in the GHz range using the low-cost and low-power CMOS technology.

Frequency synthesizer (FS) is important part of the automotive radar system.Low phase noise and high spectrum purity arevital for its good performance. Frequency synthesizer performs down-conversion and up-conversion operations in automotive radar system. Frequency synthesizer is a critical block of an automotive radarsystem, and it has large power consumption since it operates at a high frequency in the automotive radar transceiver. The voltage-controlled oscillator (VCO) and the high frequency divider are the two most important building blocks of frequency synthesizer. Power consumption and channel selection of frequency synthesizer are limited by these two critical blocks.

In this thesis, we have carried a detailed analysis on the 24GHz frequency synthesizer. Thecircuit is designed using 65nm RF CMOS technology.

TheVCO is designed incurrent-reuse technique along with the NMOS cross-coupled transistors to enhance the negative resistance requirement of oscillator. Thecurrent-reuse transistors are biased in sub-threshold region to save power consumption. To improve the phase noise performance in the designed VCO the N/PMOS cross-coupled transistors operate in differential mode providing a virtual ground. This virtual ground is connected with source of NMOS cross-coupled transistors through inductor todecrease the phase noise.The inductor source tuning technique isalso implemented in place of tail current shaping transistors used in conventional VCO to decrease the phase noise.To decrease the power consumption in the proposed circuit the frequency divider is implemented with master-slave frequency divider and true-single-phase-clock(TSPC) frequency divider scheme.

In the designed circuit, the reference frequency is 100MHz, and the output frequency is24GHz-25.8GHz. The proposed frequency synthesizer showed low power consumption of 3.52mW with the supply voltage of 0.9V. The VCO also showed a low phase noise of -117dBc at a frequency of 1MHz and -138.50dBc at 10MHz. The proposed frequency synthesizer showed a low phase noise of -116.3dBc at 1MHz and-134.7dBc at 10MHz.

Chapter 1 Introduction

The development of radio detection and ranging technology has started in the late 19^{th} with thediscovery of electromagnetic waves. The first radar circuit was implemented in the Netherlands at theRotterdam harbor and demonstrated in 1904 [1]. The first radar was designed to detectand to avoidcollision between the ships.However, the first prototype was not able to provide range information. In 1935 aircraft detectionradar was implemented after that in the Second World War the use of radar is evolved and it was used for the military purpose. The radar technology has a vast commercial use.It is used inmarine navigation,geological research, air traffic control, weather forecasting, automotive speed, and collision monitoring. The advances in low cost and small size of CMOS technologies help to use radar devicescommercially into automobile and other handheld products.

1.1 Background and Motivation

Automotive radar system is the essentialpart of advanced automobile driver assistant system since it can detect vehicles position and pedestrians around the vehicle with high accuracy. As the microwave signal has the property of low error estimation, it is successful in grabbing the attention of people towardstraffic safety, and microwave radar plays an important role in

the automotive collision avoidance sensing system. In the real application environment as shown in Figure 1.1, there will be many transmission signals from other radar systems. The interference signal would cause detection error and send a wrong message, which lets the driver make a wrong judgment.

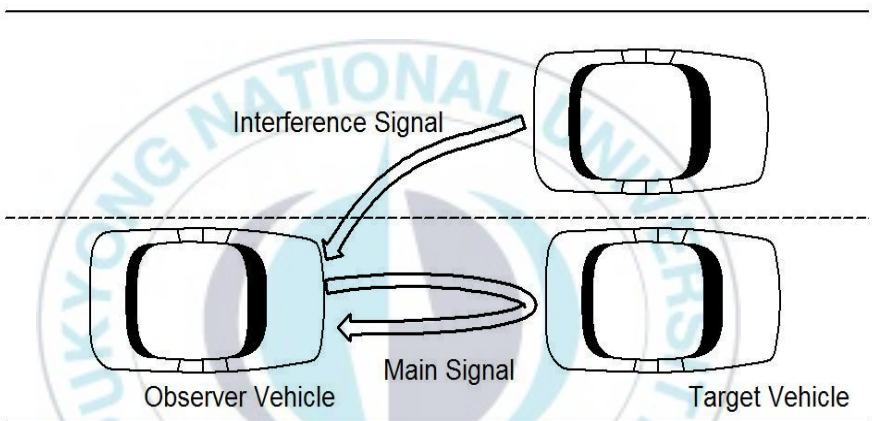


Figure 1.1 Interference in automotive radar system.

Automotive radar system includes radar frontend, analog and digital circuits, and radar signal processing software. A simple radar system design method, which includes few modeling tools and needs a little effort in parameter “synchronization” is favored.The main frequency bands of radar applications are 24GHz and 77GHz, and 24GHz is mainstream for the detection of vehicles position and pedestrians around the vehicle in the medium-short range and wide beam. For the radar system, modeling,

fabrication and echo signal synchronization has been discussed in [2]. Radar waveform and signal processing design is done in [3]. Engineering of the radar circuits is presented in [4]. The simplified radar frontend is shown in Figure 1.2. The radar is mainly made up by three parts such as frequency synthesizer, transmitter and receiver.

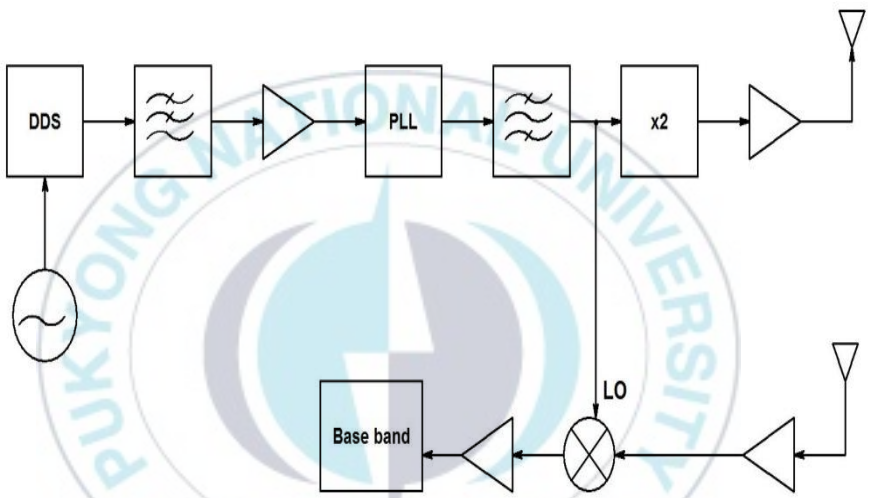


Figure 1.2 Block diagram of radar frontend.

1.2Objective of Study

The objective for this study is to develop a low-cost, low-power, low-phase noise and compact frequency synthesizer scheme operating at 24GHz-25.8GHz for automotive radar applications. This objective is achieved with the implementations of adaptivehigh speed phase frequencydetector with dead zone compensation, charge pump with infinitesimally small current mismatch, active loop filter, finely tuned and low phase noise VCO, and

low-powerfrequency divider.Frequency divider is implemented with master-slave frequency divider and TSPC frequency divider schemefor the 24GHz automotive radar system.

1.3Organization of Thesis

In chapter 2 of this thesis, we present the design of proposedphase-locked loop (PLL) based frequency synthesizers. In chapter 3,we discuss and analyze the performance andresults of the proposed frequency synthesizer. Chapter 4finally concludes the result and performance summary,and discusses the future study.

Chapter 2

Design of Frequency Synthesizer

In this chapter, we describe the concept and operating principle of a typical frequency synthesizer, and describe the design of the proposedfrequency synthesizer.

2.1 Principles and Basic Concepts for Frequency Synthesizers

A frequency synthesizer by using a clean referencesignal"f_{ref}" generates the channelized frequencies to up-convert the outgoing data for transmission and down-convert the received signal forprocessing asshown in Figure 2.1.

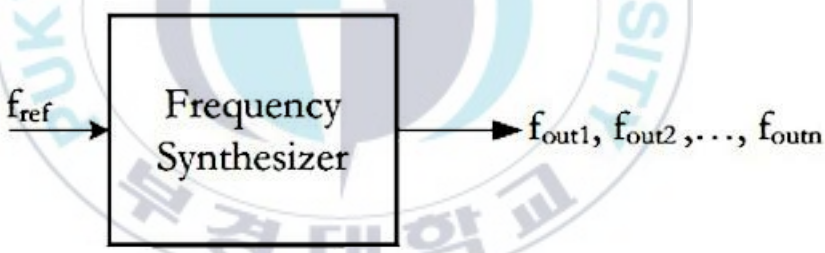


Figure 2.1Operational principleof frequency synthesizer.

A basic frequency synthesizer consists of a PLL,VCO with output frequency f_{out} and high-speed frequency divider with division ratio N as a first stage divider and a series of subsequentfrequency dividers with division ratio P . Due to the feedback operation, the output frequency of

thesynthesizeris given by

$$f_{out} = N.F.P \quad (2.1)$$

The requirements of frequency divider forRFfrequency synthesizersare much different as compared to the low frequency synthesizers. Based on thetype of frequency division ratio, the frequency synthesizer can be placed into the followingcategories.

• Integer-N frequency synthesizer, in which the division factor $N.F$ is an integer number. These frequency synthesizers are suitable for applications in whichlow resolution is required.

• Fractional-N frequency synthesizer, in which the division factor$N.F$ is a fractional number.The fractional division is achieved byemploying multi-modulus frequency dividers.

Frequency synthesizer schemes include a table-look-up synthesizer, directsynthesizer and phase-locked loop synthesizer [5].The phase-locked loop frequency synthesizer has the benefits of high frequency and low power consumption. Frequency synthesizer designed for this work also employs the phase-locked loop frequencysynthesizer architecture.

2.2 Design of Proposed Frequency Synthesizer

The block diagram of proposedphase-locked loop-based frequency synthesizer is shown in Figure2.2. The phase frequency detector (PFD) detects the difference between inputreference clock "R_{clk}" of 100MHz and the output frequency "F_{vco}" of VCO of 24GHz-25.8GHz. Theoutputs "UP" and "DN" of PFD are directly proportional to the differencebetween the input frequencies in terms ofphase and frequency. The "UP" and "DN" signals are connected with the input switches S_1 and S_2 of charge pump (CP), respectively.The CP generates the current, and the magnitude of this current is proportional to the "UP" and "DN" signals of PFD. This currentis low-pass filtered by a loop filter. This filtered signal acts as a control voltage, and controls theoutput frequency and tuning range of a VCO. The frequency divider (FD) divides the output frequency of the VCO and feedbacks this frequency to the PFD to compare with the input reference signal.

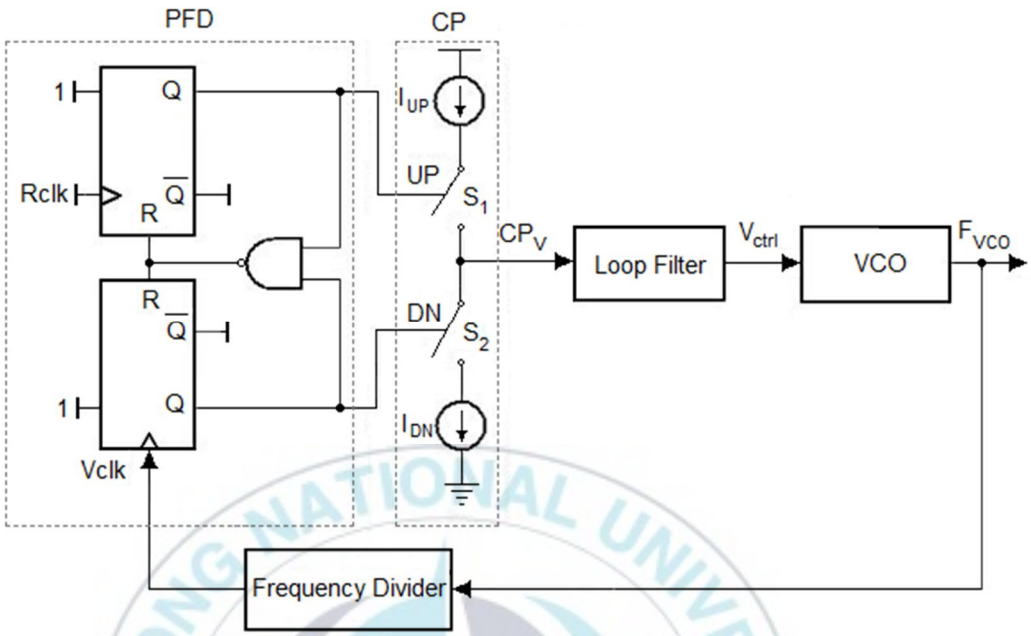


Figure 2.2Block diagram of proposed frequency synthesizer.

2.2.1Design of Phase-Locked Loop

Phase-lockedloopsare very well suited for integration in a low-cost low-power CMOS processes.PLL is very effective in the suppression of spurs and jitters, and it also has very low power dissipation.Due to these benefits of PLL, it has used inalmost all communicationchips[6].In the frequency synthesizer design, a large loop bandwidth is required. In conventional PLL design theloop bandwidth is equals to 1/10th of reference frequency. This loop bandwidth is necessary for closed loop stability of the frequency synthesizer.

2.2.2Design of Phase Frequency Detector

The PFD detects the phase and frequency difference in between the input clock signals. The proposed PFD isshown in Figure2.3. This circuit has simple structure and small dimension devices,and provides more stable operation with respect to input signal variations.In the designed PFD the number of transistors arereducedas compared to other recently usedPFDstructures[7].

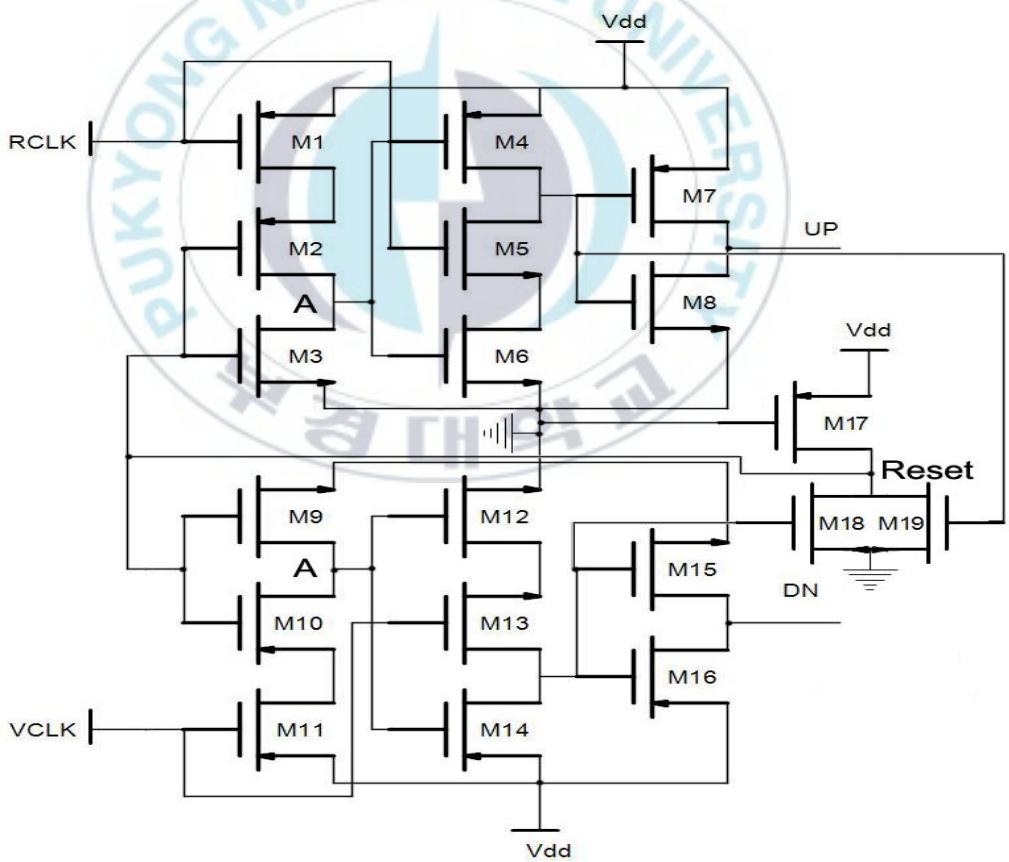


Figure2.3Design of phase frequency detector.

The circuit of proposed PFD is designed with modified TSPC flip-flop. The operation of proposed PFDis very simple.When inputs clocks "R_{clk}" and "V_{clk}" at input node, and "Reset" signals are low, the node "A"is connected to supply voltages "V_{dd}" through transistorsM1, M2, M10 and M11, and charges the node "A" to "V_{dd}". At the rising edge of inputs, the output nodeis connected to ground through M5, M6, M12 and M13. Once the node "A" is charged to "V_{dd}", the output node is not affected by input clock signal, because the charges at node "A" turn off the transistorsM5 and M13.This prevents the output nodefrom pulled up. Therefore,the output node is disconnected from input node.When the reset signal is high, node"A" is disconnected from "V_{dd}"through transistors M2 and M10, andconnected to ground throughM3 and M9. As soon as the node "A"is discharged, the output node is pulled up through M4 and M14. The M2 and M10 transistors are added to prevent the short circuit thathappens whenever the "Reset" signal is high. Moreover, the reset time is increased, because M1 and M11 charge the node "A" to "V_{dd}" while the M3 and M9 discharges node "A" to ground. Fast discharging node "A" means the fast reset operation.When the reference input clock "R_{clk}" is exceeded in phase or frequency, than the output signal"UP" will be high, and when thefeed-backed divider signal "V_{clk}" is exceeded in phase or frequency,

signal"DN"will be high.In the proposedPFD, dynamic power consumption is reduced by lowering the internal switching and speed is increased by decreasing the input to output path.

2.2.3 Design of Charge Pump

Charge pump (CP) acts as an electronic switch. It also delivers current to the loop filter,and the magnitude of the current is proportional to the output signals"UP" and "DN" of PFD[8].

When PLL is in lock condition, the magnitude of current output by the charge pump is constant. Ideally, in lock state, the current produced by CP due to the output signals "UP" and "DN" of PFD is equal in magnitude but opposite in polarities. Thus, the total current is zero and the charge pump acts as an opencircuit.Theproposed charge pump isshown in Figure 2.4.

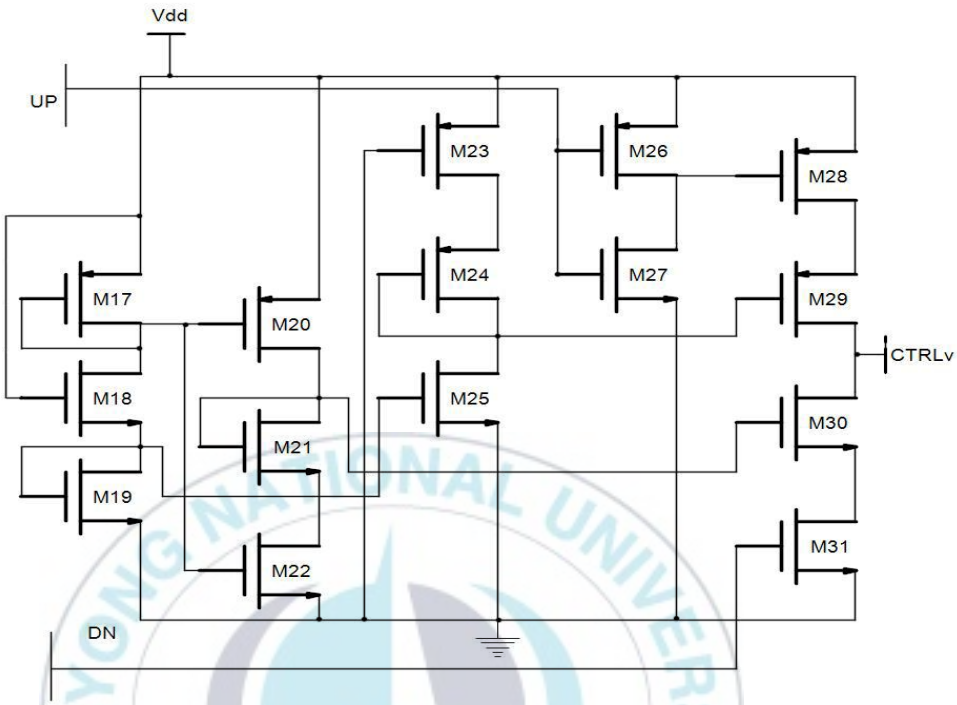


Figure 2.4 Design of charge pump.

The operation of adesigned CP is similar to the conventional tri-state chargepump. The stand-by currentsource is added in the designed charge pump to enhance the operational speed and to eliminate the high impedance state in the conventional chargepump. The stand by current does not affect theoutput current of CP. In the designed circuitthe transistors M17, M19, M21, and M24 provide the biasing current for stand-by current sourcesM20, M25, M30, and M29. The output path has small number of switching states since the current mismatchcaused by path delay mismatch can bereduced.

2.2.4Design of Loop Filter

The output of CP consists of "dc" component and the "ac" component. This "ac" outputcomponent is composed of high frequencies. The loop filter filters out these high frequencies. The loop filter integrates the discrete CP output signal. Loop filter defines the loop bandwidth of the PLL, which has significant effects on the capture range and jitters. Principally the loop filter controls the dynamic characteristics of the PLL. Figure 2.5 showsdesign of proposed active loop filter.

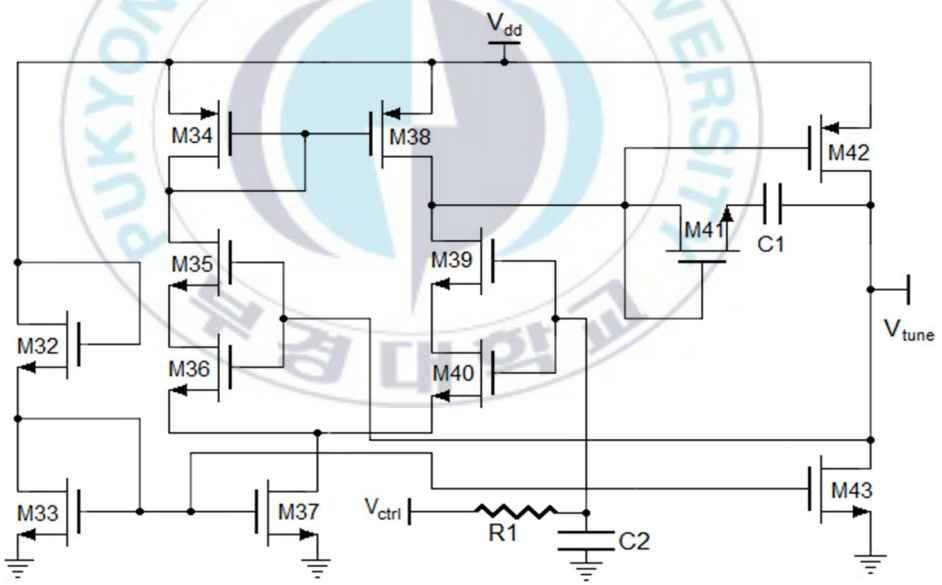


Figure2.5 Design of loop filter.

In the designed LPFthe cascoded transistors M35, M36, M39 and M40are a series connection of two conventional MOSFET, andwith an appropriate aspect ratio, these transistorsoperate as a single long channel

transistor.These transistors operate in a saturation regionwithout severe channel-length modulation effects [9].TransistorsM39 and M40are at non-inverting node of LPF, and feedback loopis connected at the inverting node with the transistors M35 and M36.TransistorsM34 and M38 are the current mirrors. The output of the first stage is the input of the secondcascaded stage. The second stage provides additional gain. Consisting of transistors M42 and M43, this stage takes the output from the drain of M39 and amplifies it through transistor M42, which is in the standard common source configuration. TransistorM43 serves as the load resistance for M42. The biasing of the LPF is achieved by using transistors M32 and M33. Capacitor C1 acts as "Millers compensation" capacitor[10].

2.2.5Design of Voltage-Controlled Oscillator

Voltage-controlled oscillator (VCO) is the most important component of the frequency synthesizer sinceit provides the actual oscillation frequency, and it defines some of the most important performance parameters of the frequency synthesizer. For instance, the tuning range of the VCO determines the range of frequencies generated by the frequency synthesizer. Similarly, phase noise of the VCO dominates the overall phase noise offrequency synthesizer. The spectral purity of the frequency synthesizer is also

dependent on the VCO. Another important contribution of the VCO is the power consumption in the overall power budget of the frequency synthesizer. Therefore, it is evident that aneffective VCO design can ensure a good frequency synthesizer.

The Schematics of different VCOs are shown inFigure 2.6.The current-reuse VCO requires less power for starting up the oscillation as compared to traditional cross-coupled VCO. In current-reuse scheme the switching of PMOS and NMOS transistors generates negative resistance to compensate the losses of tank circuit. Due to the difference of transconductance and parasitic capacitance of the PMOS and NMOS transistors, this scheme shows the variation in the differential output signals in terms of amplitude and phase[11].However, source-degeneratedcurrent-reusescheme with a negative resistance can solve this problem and increases the symmetry of the differential output signals.

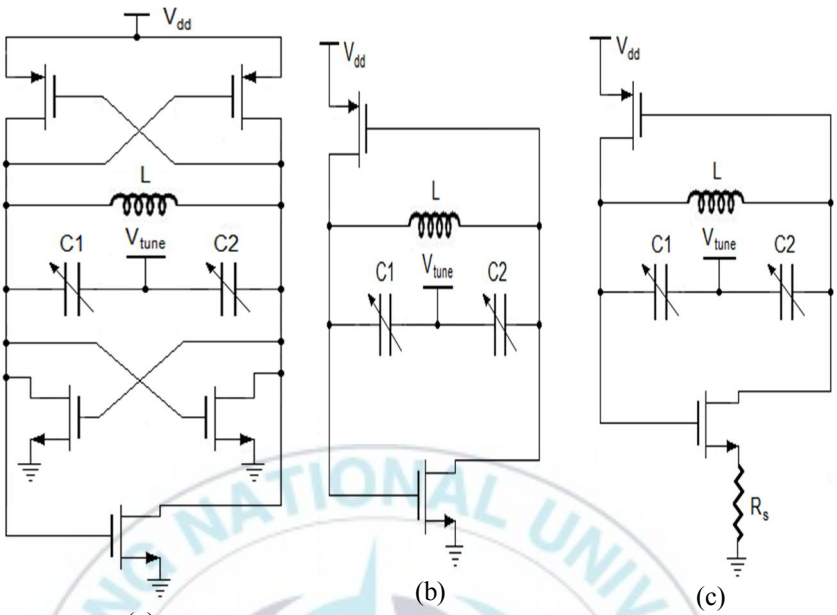


Figure 2.6 Schematics of VCOs, (a) traditional cross-coupled VCO, (b) traditional current-reuse VCO,and (c) traditional current-reuse VCO with source degeneration resistance.

The proposed VCO is shown in Figure 2.7. The VCO is designed with modified current-reuse scheme. The current-reuse scheme is modified with the implementation of NMOS cross-coupled transistorscascoded with the N/PMOS transistors of current-reuse scheme.This modified current-reuse schemeenhances the negative resistance for LC tank circuitand increases the transconductance of the VCO.To decrease the phase noise and power consumption in the designed VCO, the N/PMOS cross-coupled transistors

are biased in sub-threshold region. These transistors operate in differential mode and provide a virtual ground. This virtual ground is connected with source of cascoded NMOS cross-coupled transistors through inductor, and this inductor acts as inductive source degeneration for NMOS cross-coupled transistors, and it decreases the phase noise of VCO. The usage of inductor source tuning technique in place of tail current shaping transistors helps to reduce the power dissipation and phase noise. The capacitive feedback technique in discussed [12] is also implemented to improve the voltage swing. This implemented capacitive feedback technique helps the drain voltage of M48to oscillate above than the supply voltage and the source voltage of M49 below the ground. In this VCO design, the parallel configuration of varactors with source terminals yields a large variation in the tuning frequency for a small change in voltage.

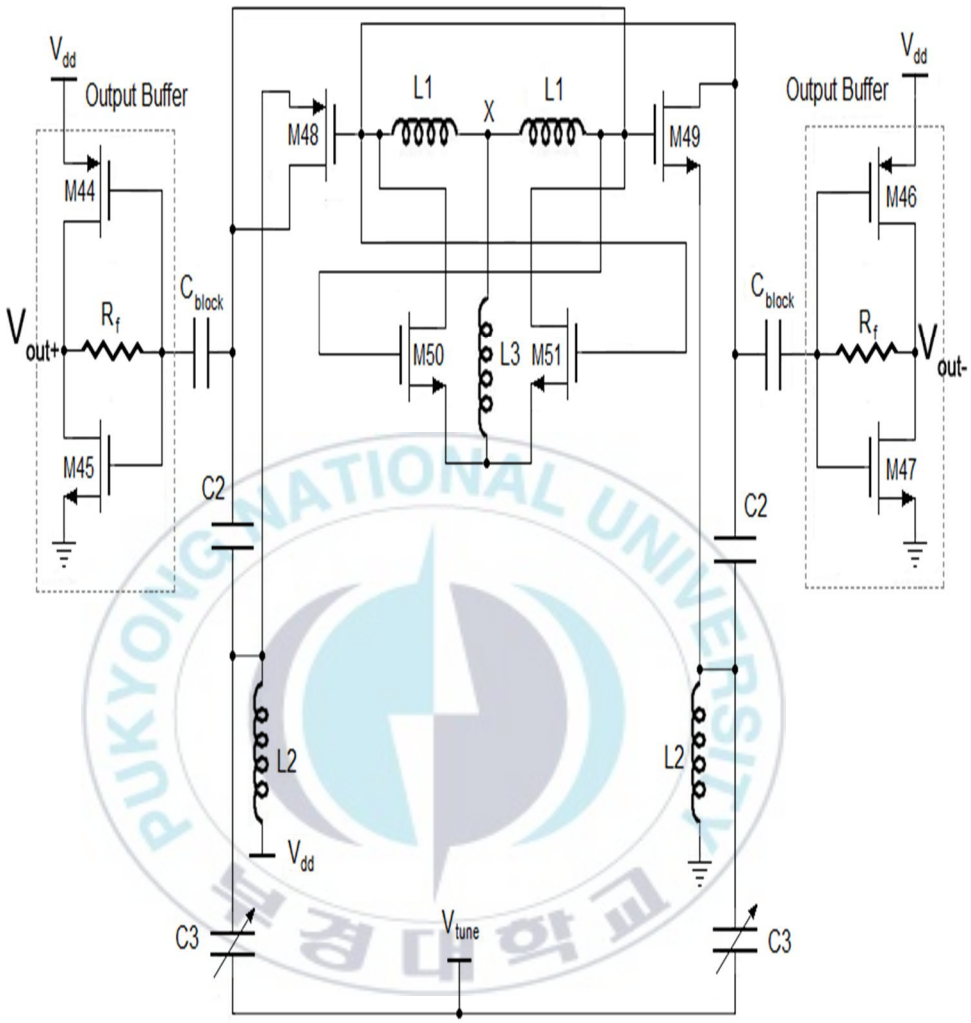


Figure 2.7Proposed VCO.

The half-circuit equivalent small-signal model of proposed VCO is depicted in Figure2.8.

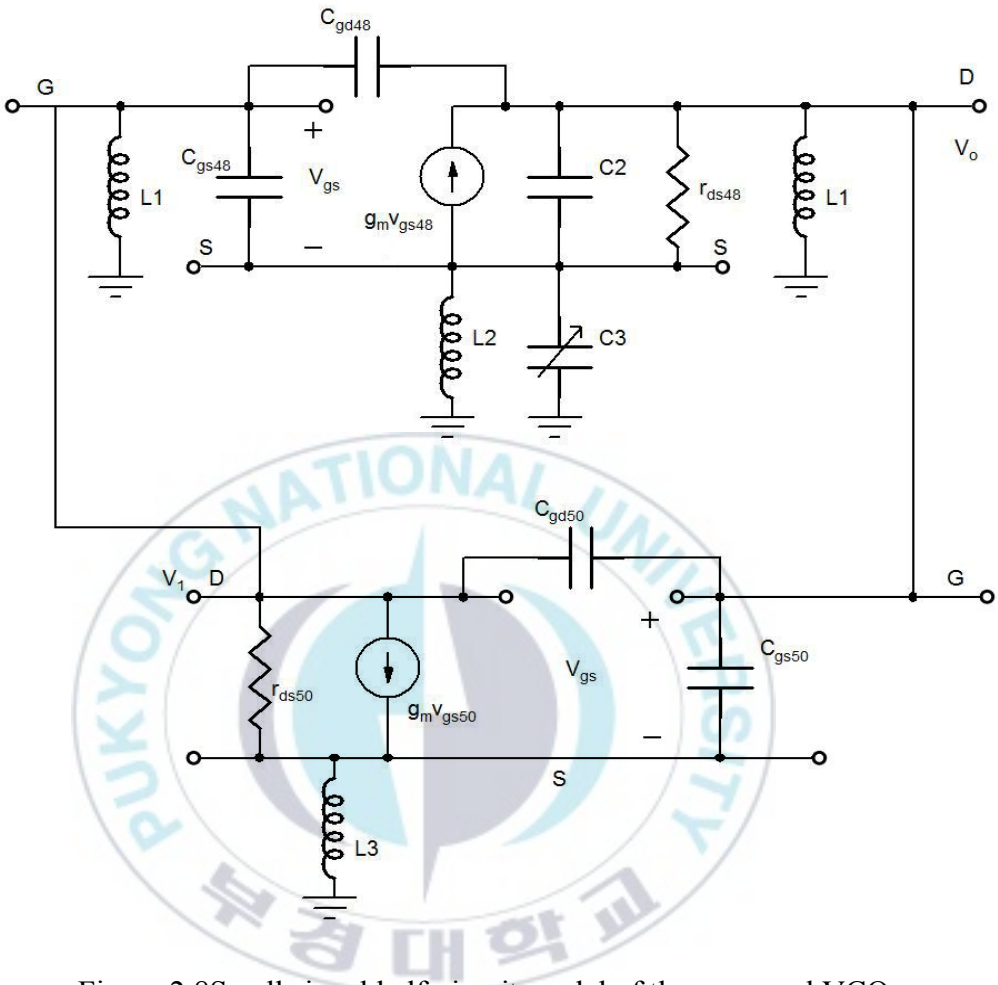


Figure 2.8Small signal half-circuit model of the proposed VCO.

In Figure 2.7 the inductors L_1 and L_2 are the LC tank inductors with losses R_{P1} and R_{P2} respectively, and the inductor L_3 is the source-degenerated inductor for cross-coupled NMOS transistors M50 and M51 with parasitic loss equal to R_{P3}. L_3 is connected with virtual ground node X, this virtual ground node is provided due to the differential operating mode of N/PMOS transistors M48 and M49. This source-

degeneratedinductorL_3helps in the decrease of $1/f^3$flicker noise of transistors M50 and M51.The inductorlossesR_{P1},$R_{P2}$and $R_{P3}$is equal to $R_{p1,2,3} \approx Q_{1,2,3}{}^2 r_s = \frac{(L_{1,2,3}\omega_0)^2}{r_s}$.

In half-circuit equivalent small-signal model Figure 2.8the voltage gain of transistor M50 is shown in Equation (1).

$$A_v = \frac{\left(g_{m50}\left(s^2 C_{gs50} L_3 + g_{m50} s L_3\right) + \left(sC_{gd50} - g_{m50}\right)\left(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3\right)\right)}{\left(\left(sC_{gd50}\right)\left(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3\right)\right)} \quad (2.2)$$

For detail ofEquation (2.2)seeEquation (7) in Appendix.

As $s = jw$ and $w >> 1$, and then we get

$$1 + s^2 C_{gs50} L_3 + g_{m50} s L_3 = s^2 C_{gs50} L_3 + g_{m50} s L_3. \quad (2.3)$$

The expression of A_v will be described in equation (2.4).

$$A_v = \frac{g_{m50} + sC_{gd50} - g_{m50}}{sC_{gd50}} = 1 \quad (2.4)$$

From $A_v = 1$,we conclude that the NMOS transistor M50 only provides the negative-resistance in the designed VCO. And the small signal voltage gain of proposed VCO is shown in Equation (2.5)

$$A_V = \frac{V_o}{V_i} = \frac{g_{m48} + sC_{gd48} - \frac{(sC_{gs48} - g_{m48})(r_{ds48} g_{m48} - sC_2 r_{ds48} - 1)}{r_{ds48} s(C_2 + C_3 + C_{gs48}) + 1 + \frac{r_{ds48}}{sL_2} - r_{ds48} g_{m48}} + \frac{sC_{gs50}}{1 + g_{m50} r_{ds50} + sC_{gs50} r_{ds50} + \frac{r_{ds50}}{sL_3}}}{\frac{(1 + r_{ds48} sC_2)(r_{ds48} g_{m48} - r_{ds48} sC_2 - 1)}{r_{ds48}{}^2 s(C_2 + C_3 + C_{gs48}) + r_{ds48} + \frac{r_{ds48}{}^2}{sL_2} - r_{ds48}{}^2 g_{m48}} - \frac{(g_{m50} + sC_{gs50}) sC_{gs50}}{\frac{1}{r_{ds50}} + g_{m50} + sC_{gs50} + \frac{1}{sL_3}} - \left(s\left(C_2 + C_{gd48} + \frac{sC_{gd50}(A_n - 1)}{A_n} + C_{gs50}\right) + \frac{1}{r_{ds48}} + \frac{1}{sL_1}\right)} \quad (2.5)$$

For detail of Equation (2.5) see Equation (25) in Appendix.

On neglecting the parasitic capacitive components and inserting$r_{ds50} \approx \infty$ in Equation (2.5)we get

$$A_V = \frac{sg_{m48}(s^2(C_2+C_3)+\frac{1}{L_2}-sg_{m48})+sg_{m48}(g_{m48}-sC_2)}{(s^3C_2)(g_{m48}-sC_2)-(s^2(C_2+C_3)+\frac{1}{L_2}-sg_{m48})(s^2C_2+\frac{1}{L_1})} \quad (2.6)$$

For detail of Equation (2.6) see Equation (27.4) in Appendix.

Now by inserting $s = jw$ in Equation (2.6) and equating $A_V = 1$ we get

$$w^4\left(2{C_2}^2 + C_2C_3\right) + w^3\left(jg_{m48}(C_2 - C_3) + w^2\left({g_{m48}}^2 + C_2g_{m48} - \frac{C_2}{L_2} - \frac{C_2}{L_1} - \frac{C_3}{L_1}\right) + w\left(\frac{jg_{m48}}{L_2} - \frac{jg_{m48}}{L_1}\right) + \left({g_{m48}}^2 - \frac{1}{L_2L_1}\right) = 0 \quad (2.7)$$

For detail of Equation (2.7) see Equation (32) in Appendix.

On equating the imaginary part equal to zero from Equation (2.7) we get the expression of oscillation frequency.

$$w = \sqrt{\frac{(L_1-L_2)}{L_2L_1(C_2-C_3)}} \quad (2.8)$$

For detail of Equation (2.8) see Equation (33) in Appendix.

On equating the real part equal to 1 from Equation (2.7) we get the start-up condition of required transconductance for proposed VCO.

$$w^4\left(2{C_2}^2 + C_2C_3\right) + w^2\left({g_{m48}}^2 + C_2g_{m48} - \frac{C_2}{L_2} - \frac{C_2}{L_1} - \frac{C_3}{L_1}\right) + \left({g_{m48}}^2 - \frac{1}{L_2L_1}\right) = 1 \quad (2.9)$$

While $w = \sqrt{\frac{(L_1-L_2)}{L_2L_1(C_2-C_3)}}$.

The figure of merit (FOM) of proposed VCO is defined in Equation (2.10).

$$FOM^T = \mathcal{L}(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\cdot\frac{F_T}{10}\right) + 10\log\left(\frac{P}{1mW}\right) \quad (2.10)$$

In Equation (9) $\mathcal{L}$ ($\Delta\omega$) represents the phase noise, and F_T represents tuning range percent.

2.2.6Design of Frequency Divider

The design of frequency synthesizer is very important and critical. The selection of a frequency divider for 24GHz-25.8GHzfrequency synthesizer needs careful consideration. Frequency divider should be able to cover the complete VCO tuning range,and it should be able to providecompensation due to the variations because of atmospheric variables.

In the traditional 24GHz frequency synthesizers, injection locked frequency divider (ILFD) and current mode logic (CML)frequency divider are used as a first stage of high frequency divider. The ILFD and CML frequency dividers operate on high speed and the maximum operating frequency of these frequency dividers is several GHz. However, the ILFD and CML frequency dividers also have high power consumption, and these frequency dividers occupy a large chip area. In the trade-off between the high speed, high power consumption and large chip area, we designed the frequency divider thatemploys two D-type latches in amaster-slave configuration with a negative feedback as afirst stage ofhighfrequency divider[13]. The operational speed ofmaster-slave frequency divider is less as compared to ILFD and CML frequency dividers, but the power consumption and chip area ofthemaster-slave frequency divider is very small.

The conventional master-slave divider includes PMOS transistors in the signal path to drive the master latch and to slave latch with a single input signal.These PMOS transistors in the signal path result in decreasing in the maximum speed of the master-slave divider. To avoid this difficulty, the proposed master-slave dividerincludes two identical D-type latches that can be driven by complementary VCO output signals of"F_{vco}" and "$\overline{F_{vco}}$".The proposed first stage of frequency divider for high frequency is shown in Figure2.9.

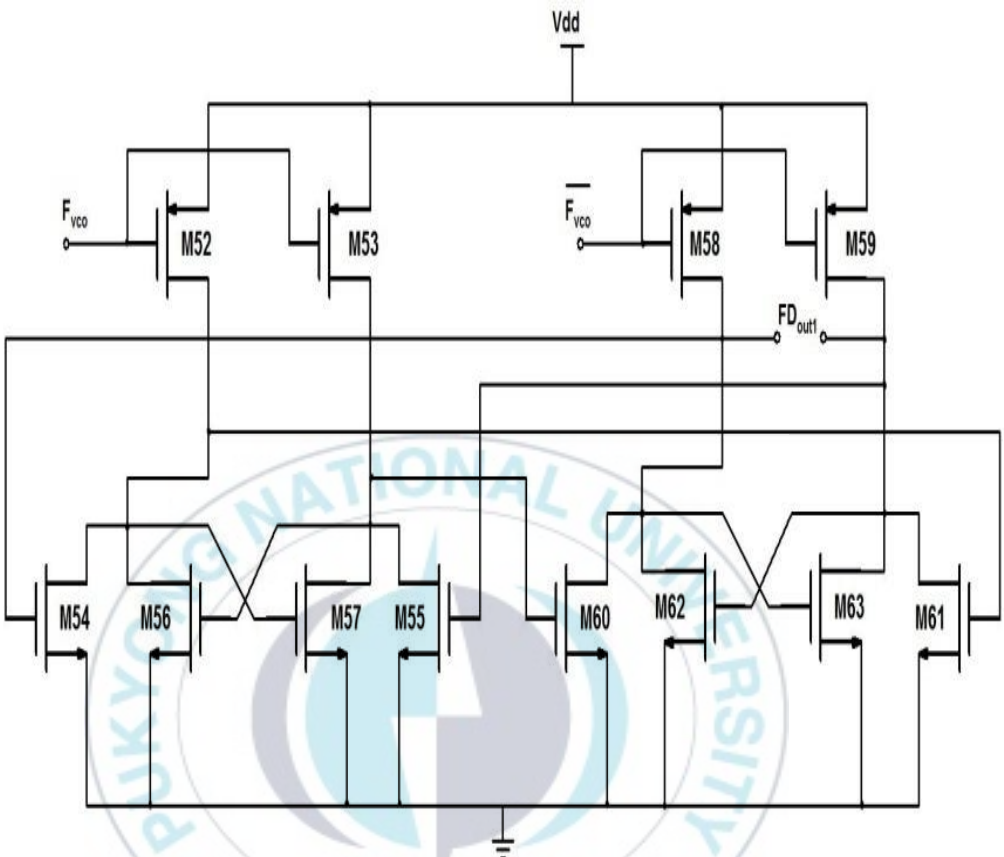


Figure2.9Proposed high frequency divider.

In the master-slave frequency divider each latch consists of transistors M54 and M55 in the masterlatch and M60 and M61 in the slavelatch to sense the signal, and transistors M56 and M57in the masterlatch and M62 and M63 in the slavelatch formed by a regenerative loop. The transistorsM52 and M53 act as pull-up transistorsin the masterlatch, and the transistors M58 and M59act as pull-up transistorsin the slavelatch.

When"F_{vco}" is in high state, transistor M52 and M53are off state, and the masterlatch operates in the sense mode. When the transistors M58 and M59 are on state the slavelatch operates in the store mode. However, when "F_{vco}"goes low,the masterlatch operates in thestore mode and slave latch operates in the sense mode.Whenever master and slavelatchesare in the sense mode, the output of masterlatch and slavelatch cannot go from low state to high statedue to the PMOS transistors.

For the low frequency stagesin thedesigned frequency divider, thetrue-single-phase-clock (TSPC) divider[14] is used to further divide the output of master-slave frequency divider and to get the low frequency equal to 100MHz. This frequency of 100MHz of TSPC divider is feedback to the PFD for the phase error detection between the input "R_{clk}" signal and output "F_{vco}" signal of FS. The TSPC divider is shown in Figure 2.10.

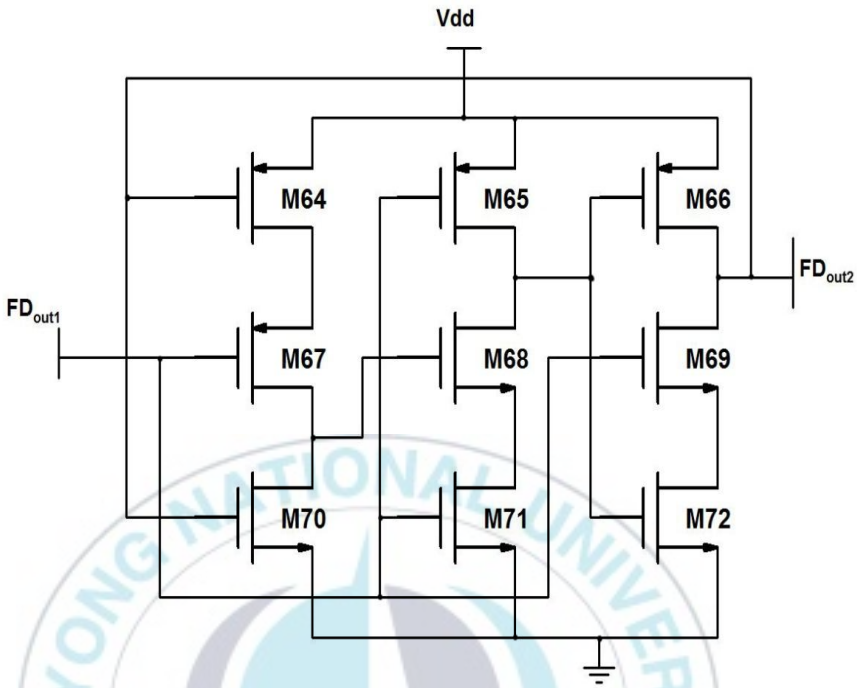


Figure2.10Proposed TSPC divider.

Chapter 3
Results and Analysis

Simulation results of proposed frequency synthesizer are realized by using the65nm RF CMOS process with the supply voltage of 0.9V. The input reference frequency for the FS is 100MHz, and the required output frequency is 24GHz-25.8GHz.

3.1 Phase Frequency Detector and Charge Pump

The transient simulation results of proposedPFD and CP at 100MHz with periodic fix phase difference of 90^0 isshown in Figure 3.1, also Figure 3.2 showsthe transient simulation results of proposedPFDand CP at 100MHz with non-periodic phase difference. The input reference signal"R_{clk}" is leading in phase by 90^0 and the output signal" V_{clk}" of frequency divider is leading in phase by 90^0 inFigures 3.1(a) and 3.1(b), respectively. The output signal waveforms of the PFD at "UP" and "DN" node, and the output waveform"$CTRL_v$"of charge pump are also shown in Figure 3.1. The PFD generates the positive "UP" signal, when the "R_{clk}" signal exceeds the "V_{clk}" signal in phase and whenever the "V_{clk}" signal exceeds the positive "DN" signal in phase. The maximum and minimum magnitudes of thesegenerated"UP" and "DN" signals are nearly equal to the rail-to-rail

supply voltages, and the magnitude of "$CTRL_v$" is proportional to these "UP" and "DN"signals. In the designed PFD, the dead zone isreduced to 0.15ns.

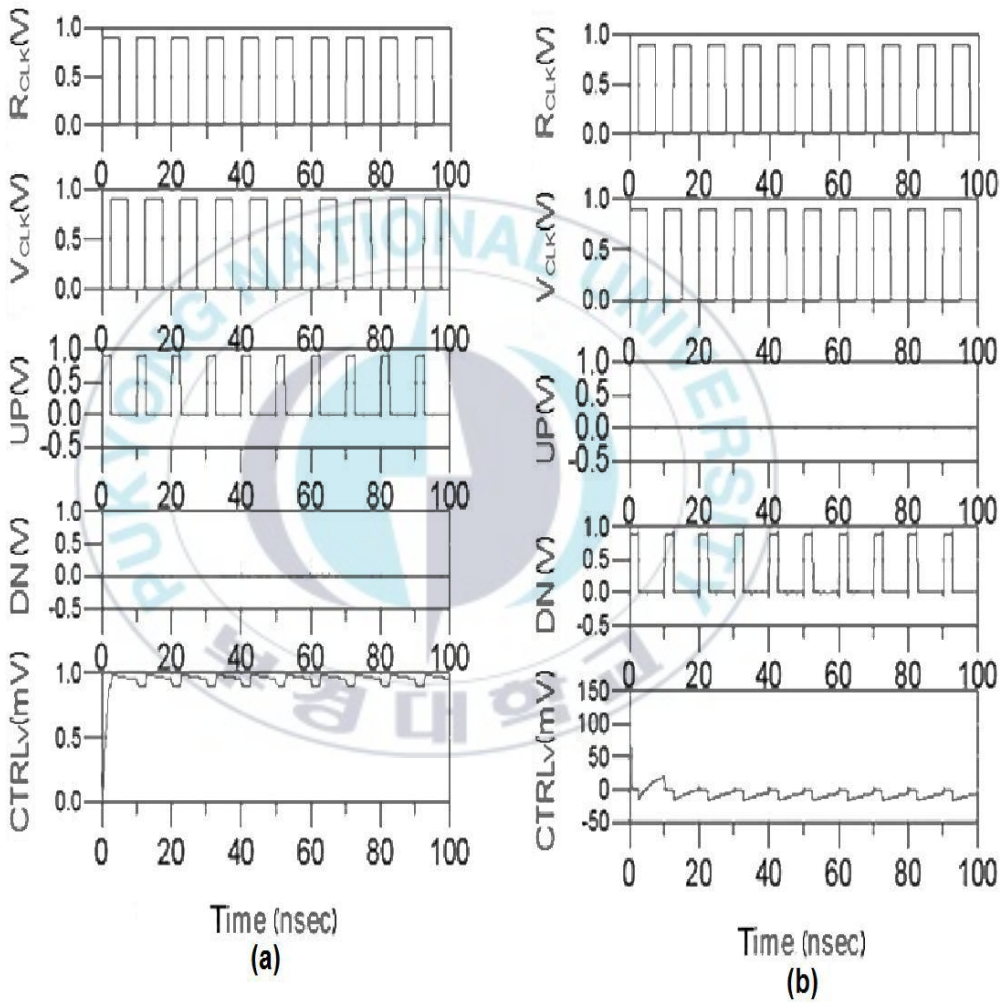


Figure 3.1Timing diagram of PFD and CP at 100MHz with periodic fix phase difference, (a) R_{clk} leading in phase, (b)V_{clk} leading in phase.

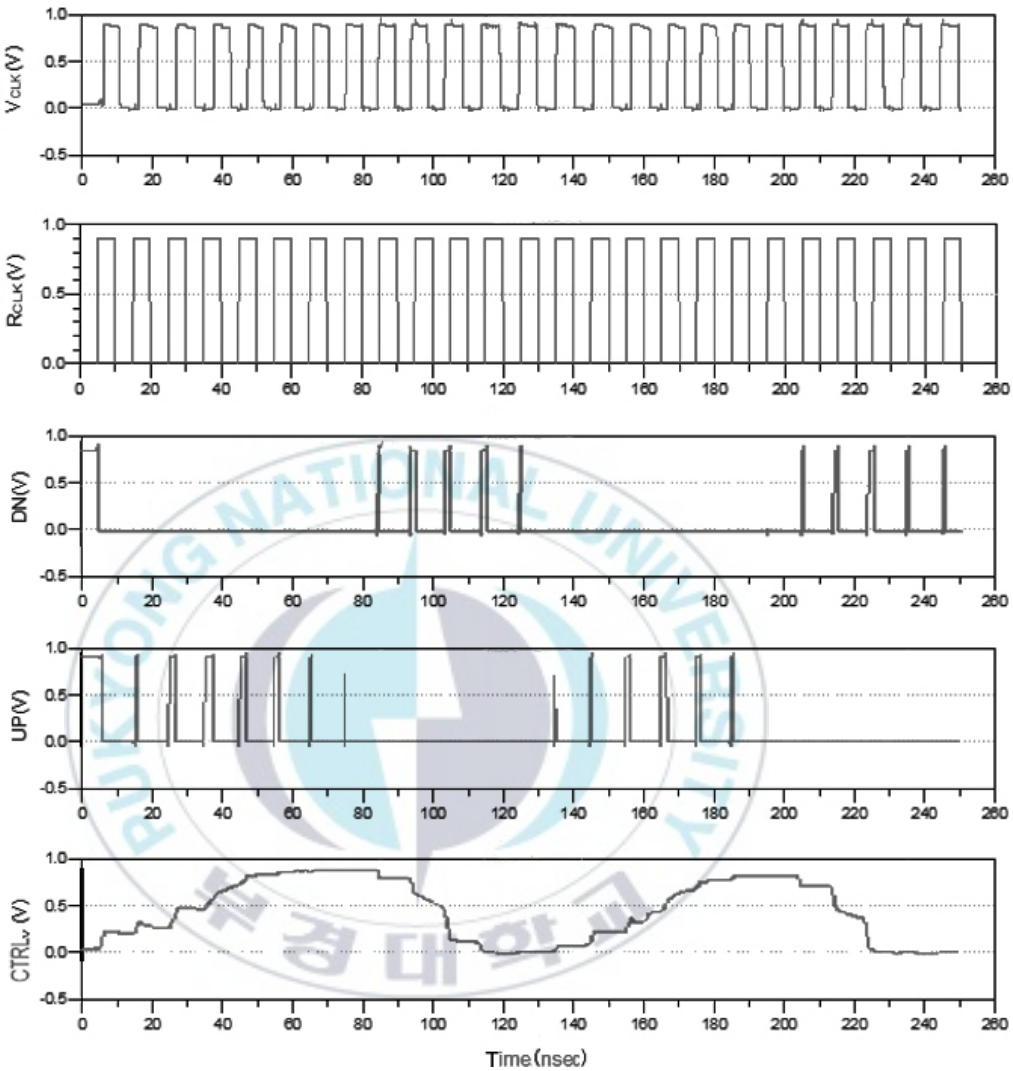


Figure 3.2 Timing diagram of PFD and CPwithnon-periodic phase difference.

3.2 Loop Filter

The unity gain of the designed LPF is shown in Figure 3.3. For low frequencies the gain is flat and equal to 0dB. Designed LPF allow low

frequencies to pass until -3dB Cut-off Frequency "F_c" which is equal to 100MHz. The simulated output signal "$CTRL_v$" of CP andoutput signal"V_{tune}"of LPF is shown in Figure3.4.

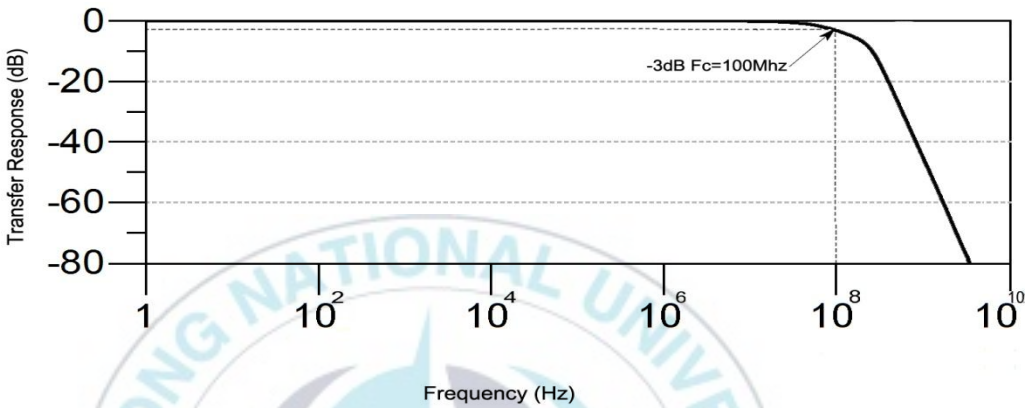


Figure 3.3 Unity gain of designed LPF.

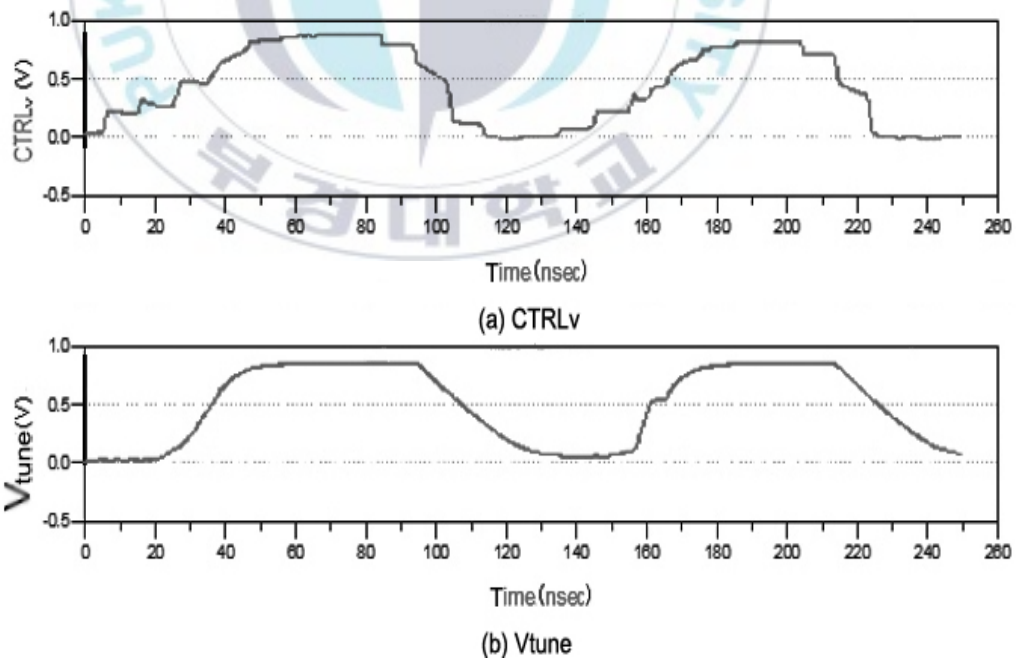


Figure 3.4 Simulated waveformof (a) CP and (b) LPF.

3.3 Voltage-Controlled Oscillator

In the proposed VCO, two output buffers in complementary push pull configuration with feedback resistor are utilized to convert the outputs of the VCO to 50Ω load for measuring results.The VCO consumes only 1.83mW with the supply voltage of 0.9V. This low power consumption is achieved due to the current-reuse scheme and inductive source-degenerated negative resistance, and due to the implementation of inductor source tunning technique.

Figure 3.5 illustrates the phase noise of the designed VCO. The designed VCO has a phase noise of -117dBc at 1MHz and -138.5dBc at 10MHz, and the VCO without inductive source degenerated negative resistance has a phase noise of -112.8dBc at 1MHz and -133.8dBc at 10MHz. As shown in Figure 3.5, the phase noise is enhanced by 4dBc as compared VCO without inductive source degenerated negative resistance.

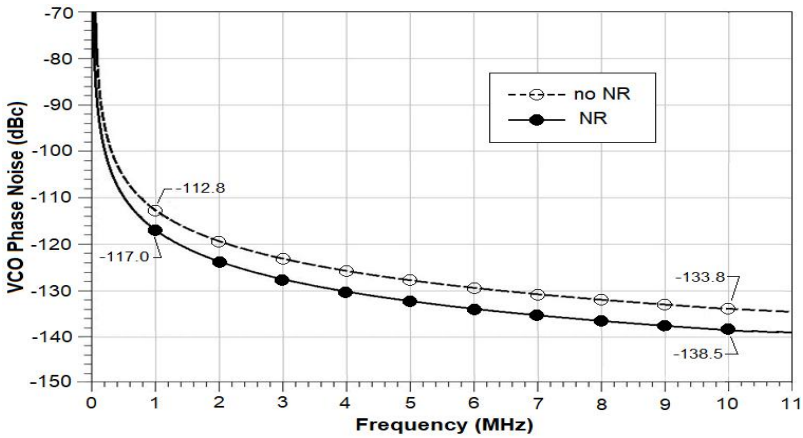


Figure 3.5 Open loop phase noise with and without negative resistance.

The symmetrical differential output waveforms "V_{out+}"and "V_{out-}", are shown in Figure 3.6. Theimplemented capacitive feedback technique in current-reuse scheme helps the drain voltage of PMOS transistor to oscillate above the supply voltage and source voltage of NMOS transistor to oscillate below the ground level.

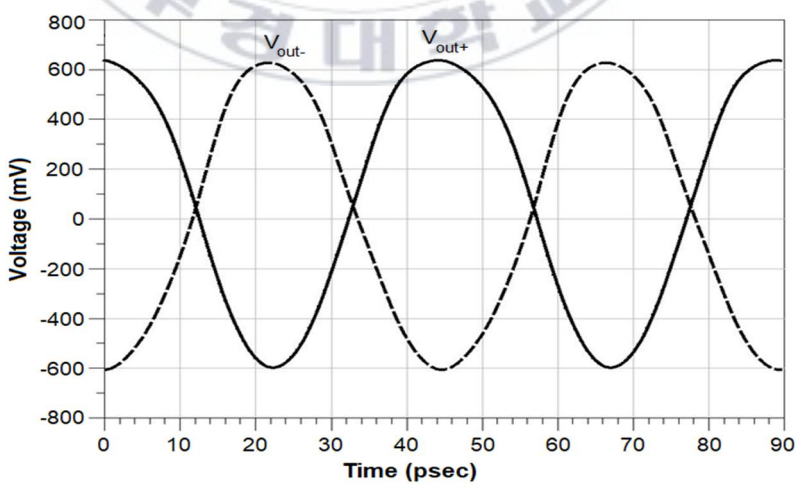


Figure3.6Differential output signals of VCO.

Figure3.7shows frequency range with respect to controlled tuned voltages for the designed VCO. The VCO showed wide frequency tunningrange of 7.5% at the frequency range of 24GHz-25.8GHz.

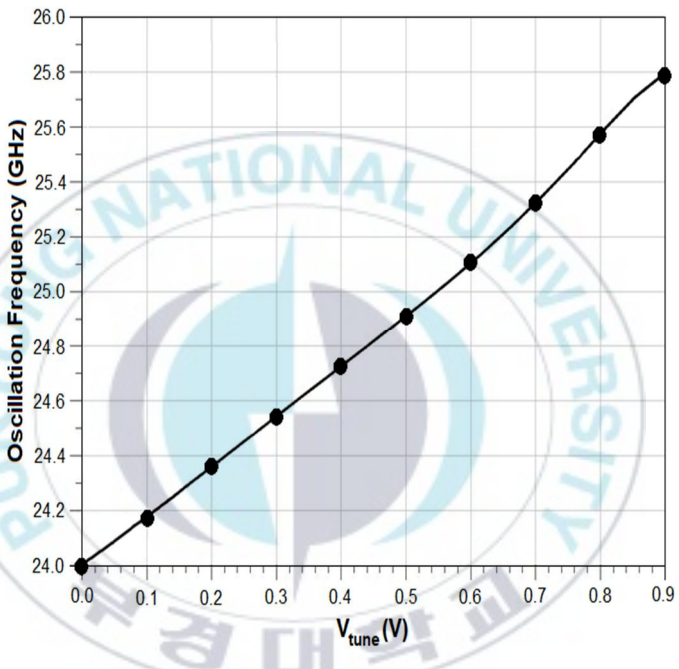


Figure3.7Frequency range vs tuning voltage.

Due to the asymmetry in the aspect ratio of N/PMOS transistor pair used in modified current-reuse scheme the start-up time of VCO is decreased [15], and the designed VCO achieved fast settling time of 3.184ns. Figure3.8shows the settling time of designed VCO.

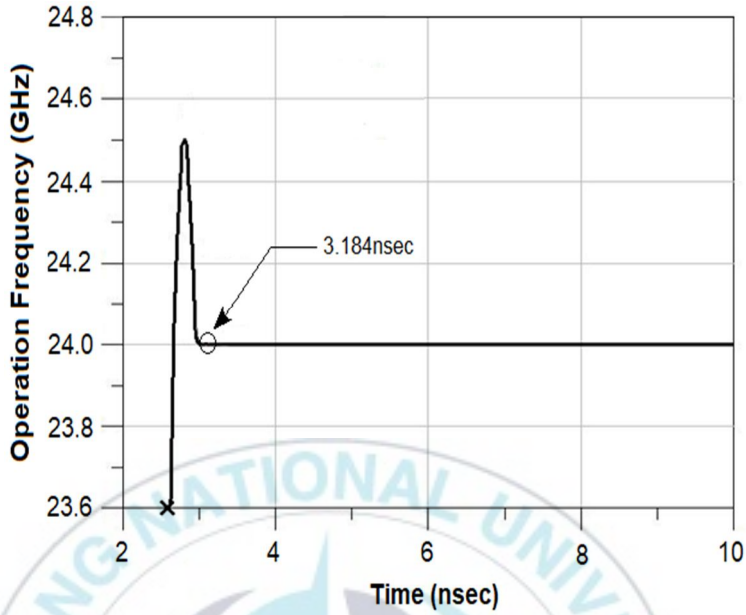
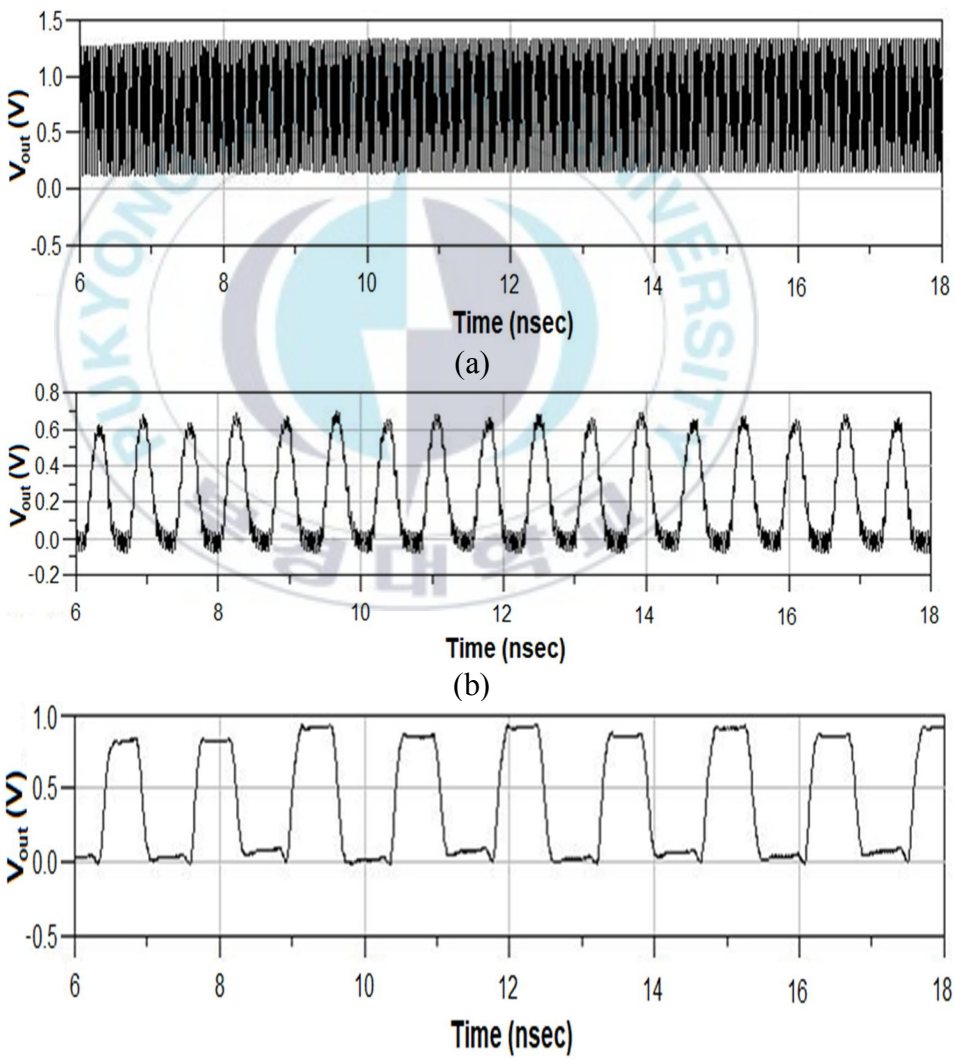


Figure3.8VCO settling time.

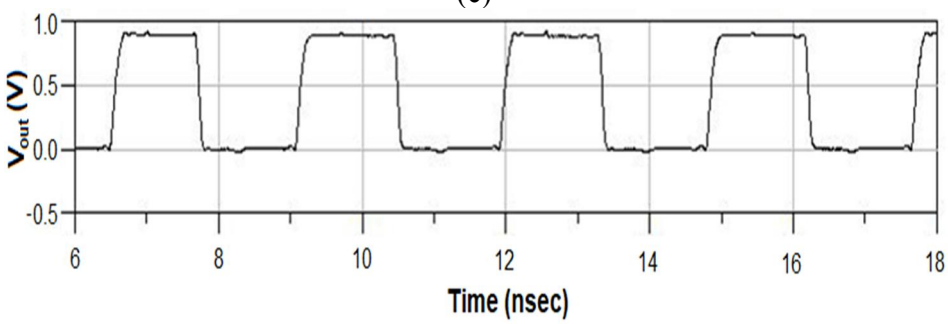
3.4 Frequency Divider

A complete transient analysis of proposed frequency divider composed of master-slave frequency divider for high frequency and TSPC frequency divider for low frequency is carried out. The frequency divider is simulated at supply voltage of 0.9V. The differential output signal "V_{out+}"and "V_{out-}" of proposed VCO are an input to the proposed high frequency master-slave frequency divider, and the low frequency output of master-slave frequency divider is given as an input to the TSPC frequency divider. The multiple blocks of the TSPC frequency divider continue the frequency division until

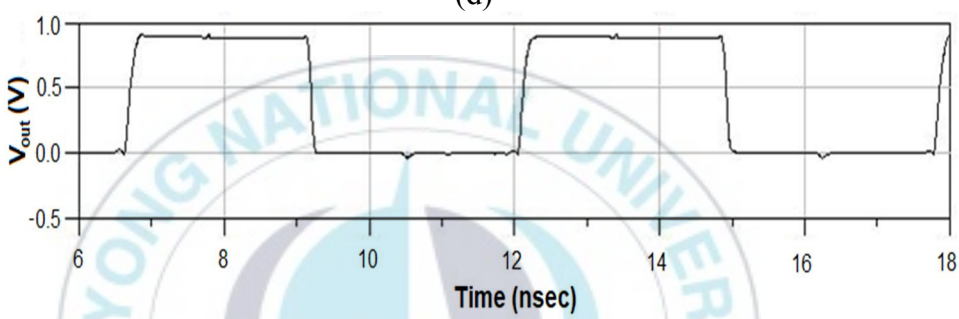
the output signal of 100MHz is achieved. This 100MHz output signal of FD is feedback to the PFD for the phase correction.Figure3.9shows input and output waveforms of master-slave frequency divider and TSPC frequency divider at different stages until the output signal of FD becomes equal to 100MHz.



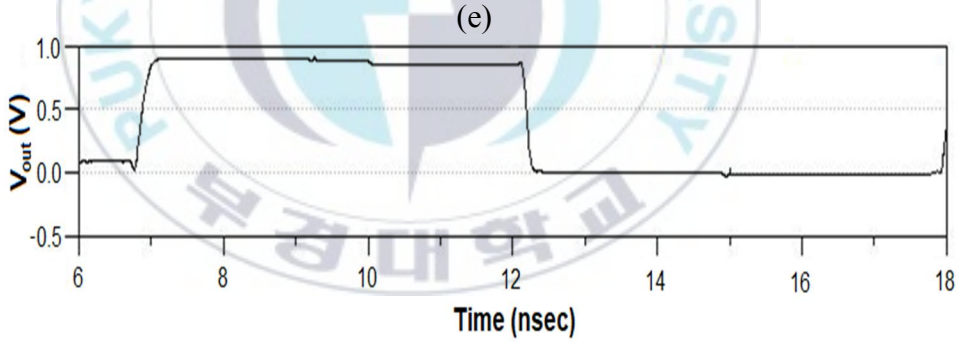
(c)



(d)



(e)



(f)

Figure3.9(a) VCO output signal of 24GHz, (b) Master-slave FD output of 1.6GHz, (c) TSPC divider output of 800MHz, (d) TSPCdivider output of 400MHz, (e) TSPC divider output of 200MHz and (f) TSPCdivider output of 100MHz.

3.5 Frequency Synthesizer

The die layout ofproposedfrequency synthesizer is shown in Figure3.10. The circuit is implemented in 65nm RF CMOS process. The size of the core cell is 0.35×0.25mm^2 and the size of die is 0.40×0.30mm^2, including a large area occupied by the wide pads.

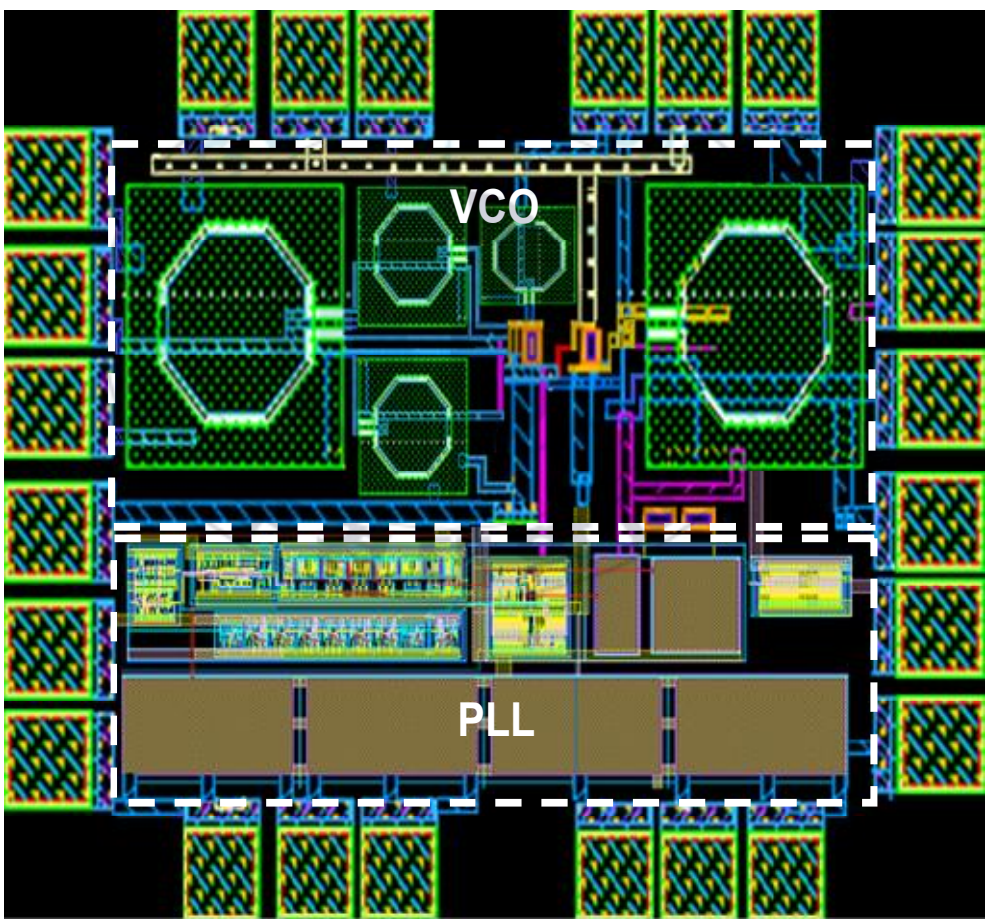


Figure3.10Dielayout.

Figure3.11illustrates the phase noise of the proposed frequency synthesizer.The measured phase noisesare-116.3dBc at the offset frequency of 1MHzand -134.7dBc at the offset frequency of 10MHz.

The closed-loop spectrum of designed FS and jitter histogram at 24GHz are shown in Figure3.12and Figure3.13, respectively. The proposed FS showed high power density of -5.36dB at the operation frequency of 24GHz. The FS also showed very low peak-to-peak jitter noise of 3.5ps, and very low rms jitter of 0.75ps.

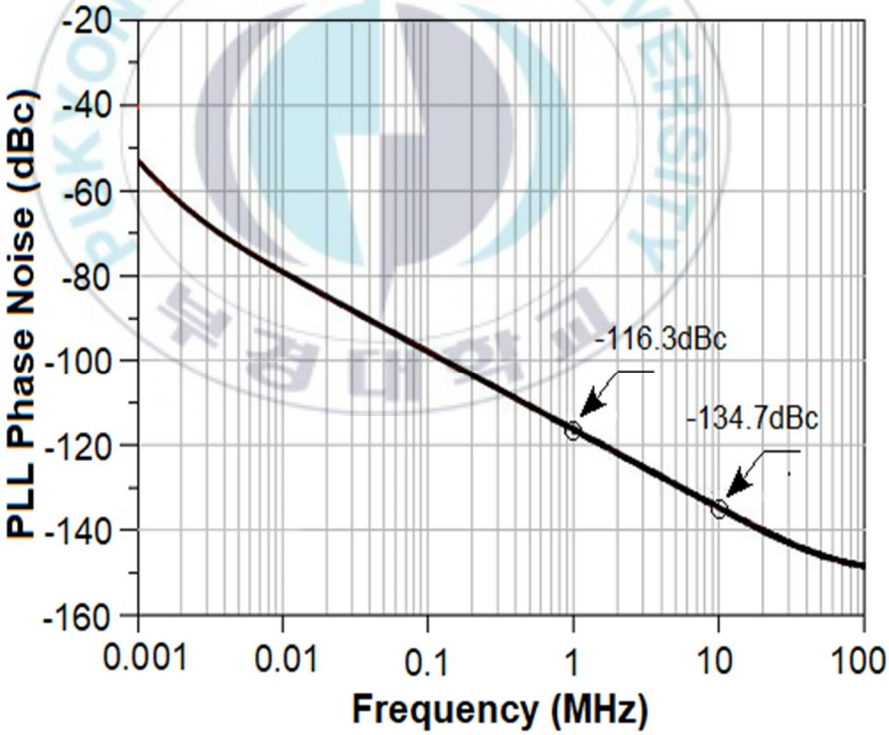


Figure3.11Closed-loop PLL phase noise.

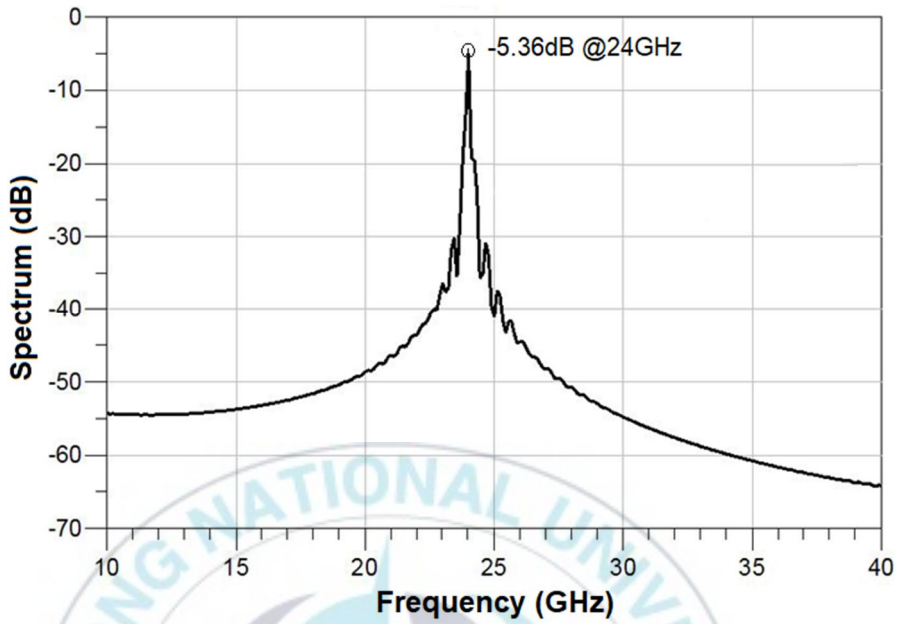


Figure3.12Closed-loop spectrum.

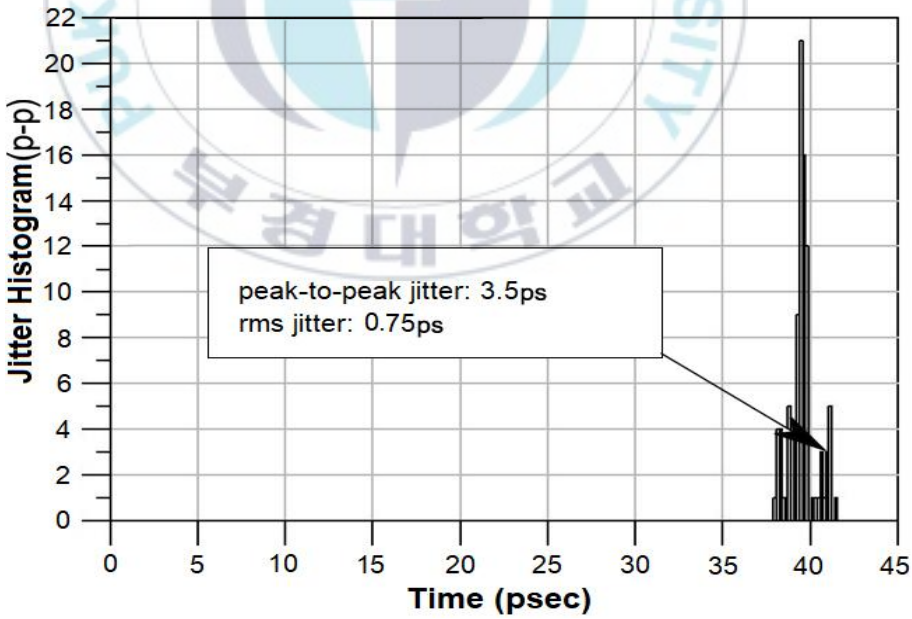


Figure3.13Jitter histogram.

The percentage of power consumed by each block of FS is shown in Figure 3.14. The VCO provided power dissipation of more than 50% as expected. The PLL dissipated power of 48%, and frequency divider consisting of master-slave FD and TSPC FD showed power dissipation of more than 50% in PLL.

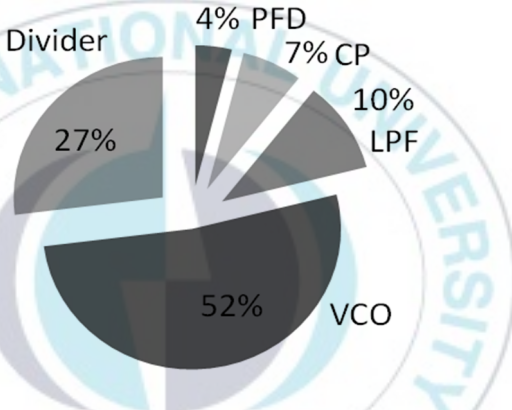


Figure3.14Power consumption.

Table 1 summarize the performance comparison of the proposed frequency synthesizer with three previously published papers, with output frequencies around 20 GHz to 24GHz. From the Table 1 it visible that the proposed FS achieves a noticeable good results in power consumption which is only3.52mWand phase noise of -116.95 at 1MHz and -138.5 at 10MHz as compared to [16],[17] and [18]. The major reason due to which

[16],[17] and [18] have higher power consumption is due to the use of ILFD and CML, based frequency dividers. While in the proposed FS the master-slave frequency divider is used, which is slow in speed as compared to ILFD and CML but the power consumption of master-slave frequency divider is also very less as compared to ILFD and CML. The second reason due to which the proposed FS showed a low phase noise and a low power consumption is the implementation of novel modified current-reuse VCO, becausethe transistors in current-reuse VCO are only switched on in the first half of period, which greatly reduces the power dissipation [19].

Table 1. Summary and comparison of FS performance

Parameters	**[16]**	**[17]**	**[18]**	**This Work**
Technology (nm)	90	180	180	65
Output Frequency (GHz)	20	24.37	24.2	24
Reference Frequency(GHz)	0.3125	0.4	12.1	0.1
Supply Voltage (V)	1.3	1.2	1	0.9
Power Dissipation (mW)	38	31.6	17.5	**3.52**
VCO Phase Noise (dBc/Hz)	-113 @ 1MHz	-110 @ 1MHz	-119.3 @ 10MHz	**-116.95**@1MHz **-138.5**@10MHz
PLL Phase Noise (dBc/Hz)	-	-	-119.1 @ 10MHz	**-116.3**@1MHz **-134.7**@10MHz
Tuning Range (%)	4.7	4.73	6	**7.5**

Chapter 4Conclusions and Future Study

4.1 Conclusions

In this thesis, a fully integrated24GHz-25.8GHz frequency synthesizer for automotive radar applications are presented. The proposed frequency synthesizer is implemented in 65nm RF CMOS process.Thanks to the implementation of high speed PFD, low phase noise VCO andlow-power frequency divider the power consumption and phase noise of proposed frequency synthesizer is very low. VCO is implemented with the modifiedcurrent-reuse technique, along with the inductive source tunning technique.The VCO achieved a FOM of -199.7dB and the FS showed very low phase noisesof-116.3dBcat 1MHz and 134.7dBc at 10MHz. Due to the implementation of master-slave and TSPC divider for 24GHz-25.8GHz, instead of ILFD and CML frequency dividers, the FS showed very low power of only 3.52mW at the power supply of 0.9V.The VCO also showed wide oscillator frequency range of 7.5% and the frequency range of24GHz-25.8GHz.The FS showed very low peak-to-peak jitter noise of 3.5ps, and very low rms jitter of 0.75ps.The size of thecore cell was $0.35\times0.25mm^2$, and the size of diewas $0.40\times0.30mm^2$including pads.

4.2 Future Study

Today the automobile industries shows a great interest in the automotive radar monitoring systems, as it is the essential part of modern automobiles. Frequency synthesizers play a key functional role in the automotive radar monitoring systems. As it aids the radar system to correctly detect the environment around the vehicle and help to prevent the crashes. The translation between the 24GHz and 77GHz operating frequency bands, of automotive radar monitoring system requires a dual band frequency synthesizer to incorporate these operating frequency bands. This work only considers the 24GHz frequency band, but in future work can be done on dual band frequency synthesizer.

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[Appendix]

$$\frac{V_o - V_s}{r_{ds50}} + g_{m50} v_{gs50} + (V_o - V_s) s C_{gd50} = 0 \qquad (1)$$

By applying the KCL at source node we get

$$\left((V_g - V_s) s C_{gs50} + g_{m50} v_{gs50} + \frac{V_o - V_s}{r_{ds50}}\right) s L_3 = V_s . \qquad (2)$$

By rearranging Equation (2), we get the value of voltage V_s at source node.

$$V_s = \frac{\left(V_g (s^2 C_{gs50} L_3 + g_{m50} s L_3) + \frac{V_o s L_3}{r_{ds50}}\right)}{\left(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3 + \frac{s L_3}{r_{ds50}}\right)} \qquad (3)$$

By rearranging Equation (1) and inserting $V_{gs50} = V_{g50} - V_{s50}$,we get

$$V_o + V_{g50} g_{m50} r_{ds50} + V_o r_{ds50} s C_{gd50} - V_{g50} r_{ds50} s C_{gd50} = (1 + g_{m50} r_{ds50}) V_s . \qquad (4)$$

From Equations (3) and (4), we get

$$V_o \left(\left(1 + r_{ds50} s C_{gd50}\right) \left(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3 + \frac{s L_3}{r_{ds50}}\right) - \left(\frac{(1 + g_{m50} r_{ds50}) s L_3}{r_{ds50}}\right) \right) =$$

$$V_g \left(\left(-g_{m50} r_{ds50} + r_{ds50} s C_{gd50}\right) \left(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3 + \frac{s L_3}{r_{ds50}}\right) + (1 + g_{m50} r_{ds50})(s^2 C_{gs50} L_3 + g_{m50} s L_3) \right). \qquad (5)$$

As we assumed $V_g = V_i$ for NMOS transistor, M50 and then voltage gain of M50 is $A_v = \frac{V_o}{V_g} = \frac{V_o}{V_i}$. By rearranging Equation (5) we get Equation (6).

$$A_v = \frac{V_o}{V_g} = \frac{V_o}{V_i} =$$

$$\frac{\left(r_{ds50}(s C_{gd50} - g_{m50})\left(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3 + \frac{s L_3}{r_{ds50}}\right) + (1 + g_{m50} r_{ds50})(s^2 C_{gs50} L_3 + g_{m50} s L_3)\right)}{\left((1 + r_{ds50} s C_{gd50})\left(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3 + \frac{s L_3}{r_{ds50}}\right) - \left(\frac{(1 + g_{m50} r_{ds50}) s L_3}{r_{ds50}}\right)\right)} \qquad (6)$$

Now we analyze the gain result by inserting $r_{ds50} \approx \infty$, and we get

$$A_v = \frac{(g_{m50}(s^2 C_{gs50} L_3 + g_{m50} s L_3) + (sC_{gd50} - g_{m50})(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3))}{((sC_{gd50})(1 + s^2 C_{gs50} L_3 + g_{m50} s L_3))} (7)$$

As $s = jw$ and $w >> 1$, and then we get

$$1 + s^2 C_{gs50} L_3 + g_{m50} s L_3 = s^2 C_{gs50} L_3 + g_{m50} s L_3 . (8)$$

The expression of A_v will be described in equation (9).

$$A_v = \frac{g_{m50} + sC_{gd50} - g_{m50}}{sC_{gd50}} = 1 \quad (9)$$

$$V_i s C_{gd50}(1 - A_n) + \frac{V_i}{sL_1} + \frac{V_i - V_{s50}}{r_{ds50}} + g_{m50} v_{gs50} + (V_i - V_o) s C_{gd48} + (V_i - V_{s48}) s C_{gd48} = 0 (10)$$

$$\frac{V_i - V_{s50}}{r_{ds50}} + g_{m50} v_{gs50} + (V_o - V_{s50}) s C_{gs50} = \frac{V_{s50}}{sL_3} (11)$$

$$g_{m48} v_{gs48} + (V_i - V_o) s C_{gd48} = \frac{V_o - V_{s48}}{r_{ds48}} + \frac{V_o}{sL_1} + (V_o - V_{s50}) s C_{gs50} + \frac{V_o s C_{gd50}(A_n - 1)}{A_n} + (V_o - V_{s48}) s C_2 (12)$$

$$g_{m48} v_{gs48} + \frac{V_{s48}}{sL_2} + V_{s48} s C_3 = \frac{V_o - V_{s48}}{r_{ds48}} + (V_i - V_{s48}) s C_{gs48} + (V_o - V_{s48}) s C_2 (13)$$

As $V_i = V_{g48} = V_{d50}$, $V_o = V_{g50} = V_{d48}$, $V_{gs50} = V_{g50} - V_{s50}$ and $V_{gs48} = V_{g48} - V_{s48}$ by inserting these values and rearranging, we get V_{s50} Equation (11) and from we will get V_{s48} Equation (13).

From Equation (11), we get

$$\frac{V_{s50}}{r_{ds50}} + \frac{V_i}{r_{ds50}} + g_{m50}(V_o - V_{s50}) + V_o s C_{gs50} - V_{s50} s C_{gs50} = \frac{V_{s50}}{sL_3} (14)$$

$$V_{s50} = \frac{\frac{V_i}{r_{ds50}} + g_{m50}V_o + V_o sC_{gs50}}{\frac{1}{r_{ds50}} + g_{m50} + sC_{gs50} + \frac{1}{sL_3}} (15)$$

From Equation (13), we obtain

$$g_{m48}(V_i - V_{s48}) + \frac{V_{s48}}{sL_2} + V_{s48}sC_3 = \frac{V_o}{r_{ds48}} - \frac{V_{s48}}{r_{ds48}} + V_i sC_{gs48} - V_{s48}sC_{gs48} + V_o sC_2 - V_{s48}sC_2 (16)$$

$$V_{s48}\left(-g_{m48} + \frac{1}{sL_2} + sC_3 + \frac{1}{r_{ds48}} + sC_{gs48} + sC_2\right) = -V_i g_{m48} + \frac{V_o}{r_{ds48}} + V_i sC_{gs48} + V_o sC_2 (17)$$

$$V_{s48} = \frac{V_i sC_{gs48} - V_i g_{m48} + \frac{V_o}{r_{ds48}} + V_o sC_2}{s(C_2 + C_3) + sC_{gs48} + \frac{1}{r_{ds48}} + \frac{1}{sL_2} - g_{m48}} (18)$$

$$V_{s48} = \frac{V_i(sC_{gs48} - g_{m48}) + V_o(\frac{1}{r_{ds48}} + sC_2)}{s(C_2 + C_3 + C_{gs48}) + \frac{1}{r_{ds48}} + \frac{1}{sL_2} - g_{m48}} (19)$$

From Equation (12), we get

$$g_{m48}(V_i - V_{s48}) + (V_i - V_o)sC_{gd48} = (V_o - V_{s48})sC_2 + \frac{V_o - V_{s48}}{r_{ds48}} + \frac{V_o}{sL_1} + \frac{V_o sC_{gd50}(A_n - 1)}{A_n} + V_o sC_{gs50} - V_{s50}sC_{gs50} (20)$$

$$V_i\left(g_{m48} + sC_{gd48}\right) + V_o\left(-sC_2 - sC_{gd48} - \frac{1}{r_{ds48}} - \frac{1}{sL_1} - \frac{sC_{gd50}(A_n - 1)}{A_n} - sC_{gs50}\right) = V_{s48}\left(g_{m48} - sC_2 - \frac{1}{r_{ds48}}\right) - V_{s50}sC_{gs50} (21)$$

Inserting the values of V_{s50} and V_{s48} from Equations (15) and (19) in Equation (21) we get

$$V_i\left(g_{m48} + sC_{gd48}\right) + V_o\left(-sC_2 - sC_{gd48} - \frac{sC_{gd50}(A_n - 1)}{A_n} - \frac{1}{r_{ds48}} - \frac{1}{sL_1} - sC_{gs50}\right) = \frac{V_i(sC_{gs48} - g_{m48})\left(g_{m48} - sC_2 - \frac{1}{r_{ds48}}\right)}{s(C_2 + C_3 + C_{gs48}) + \frac{1}{r_{ds48}} + \frac{1}{sL_2} - g_{m48}} + \frac{V_o(\frac{1}{r_{ds48}} + sC_2)\left(g_{m48} - sC_2 - \frac{1}{r_{ds48}}\right)}{s(C_2 + C_3 + C_{gs48}) + \frac{1}{r_{ds48}} + \frac{1}{sL_2} - g_{m48}} - \frac{(\frac{V_i}{r_{ds50}} + g_{m50}V_o + V_o sC_{gs50})sC_{gs50}}{\frac{1}{r_{ds50}} + g_{m50} + sC_{gs50} + \frac{1}{sL_3}} (22)$$

$$V_i\left(g_{m48}+sC_{gd48}-\frac{(sC_{gs48}-g_{m48})\left(g_{m48}-sC_2-\frac{1}{r_{ds48}}\right)}{s(C_2+C_3+C_{gs48})+\frac{1}{r_{ds48}}+\frac{1}{sL_2}-g_{m48}}+\frac{sC_{gs50}}{1+g_{m50}r_{ds50}+sC_{gs50}r_{ds50}+\frac{r_{ds50}}{sL_3}}\right)=V_o\left(\frac{(\frac{1}{r_{ds48}}+sC_2)\left(g_{m48}-sC_2-\frac{1}{r_{ds48}}\right)}{s(C_2+C_3+C_{gs48})+\frac{1}{r_{ds48}}+\frac{1}{sL_2}-g_{m48}}-\right.$$

$$\left.\frac{(g_{m50}+sC_{gs50})sC_{gs50}}{\frac{1}{r_{ds50}}+g_{m50}+sC_{gs50}+\frac{1}{sL_3}}-\left(s\left(C_2+C_{gd48}+\frac{sC_{gd50}(A_n-1)}{A_n}+C_{gs50}\right)+\frac{1}{r_{ds48}}+\frac{1}{sL_1}\right)\right)(23)$$

On multiplying and dividing both sides of Equation (23) by r_{ds48} we get

$$V_i\left(g_{m48}+sC_{gd48}-\frac{(sC_{gs48}-g_{m48})(r_{ds48}g_{m48}-sC_2r_{ds48}-1)}{r_{ds48}s(C_2+C_3+C_{gs48})+1+\frac{r_{ds48}}{sL_2}-r_{ds48}g_{m48}}+\frac{sC_{gs50}}{1+g_{m50}r_{ds50}+sC_{gs50}r_{ds50}+\frac{r_{ds50}}{sL_3}}\right)=$$

$$V_o\left(\frac{(1+r_{ds48}sC_2)(r_{ds48}g_{m48}-r_{ds48}sC_2-1)}{{r_{ds48}}^2s(C_2+C_3+C_{gs48})+r_{ds48}+\frac{{r_{ds48}}^2}{sL_2}-{r_{ds48}}^2g_{m48}}-\frac{(g_{m50}+sC_{gs50})sC_{gs50}}{\frac{1}{r_{ds50}}+g_{m50}+sC_{gs50}+\frac{1}{sL_3}}-\left(s\left(C_2+C_{gd48}+\frac{sC_{gd50}(A_n-1)}{A_n}+C_{gs50}\right)+\right.\right.$$

$$\left.\left.\frac{1}{r_{ds48}}+\frac{1}{sL_1}\right)\right)(24)$$

From Equation (24), we get small signal voltage gain $(A_V=\frac{V_o}{V_i})_{|I_o=0}$ of proposed VCO.

$$A_V=\frac{V_o}{V_i}=\frac{g_{m48}+sC_{gd48}-\frac{(sC_{gs48}-g_{m48})(r_{ds48}g_{m48}-sC_2r_{ds48}-1)}{r_{ds48}s(C_2+C_3+C_{gs48})+1+\frac{r_{ds48}}{sL_2}-r_{ds48}g_{m48}}+\frac{sC_{gs50}}{1+g_{m50}r_{ds50}+sC_{gs50}r_{ds50}+\frac{r_{ds50}}{sL_3}}}{\frac{(1+r_{ds48}sC_2)(r_{ds48}g_{m48}-r_{ds48}sC_2-1)}{{r_{ds48}}^2s(C_2+C_3+C_{gs48})+r_{ds48}+\frac{{r_{ds48}}^2}{sL_2}-{r_{ds48}}^2g_{m48}}-\frac{(g_{m50}+sC_{gs50})sC_{gs50}}{\frac{1}{r_{ds50}}+g_{m50}+sC_{gs50}+\frac{1}{sL_3}}-\left(s\left(C_2+C_{gd48}+\frac{sC_{gd50}(A_n-1)}{A_n}+C_{gs50}\right)+\frac{1}{r_{ds48}}+\frac{1}{sL_1}\right)}(25)$$

On neglecting the parasitic capacitive components from the expression of A_V we get

$$A_V=\frac{g_{m48}+\frac{g_{m48}(r_{ds48}g_{m48}-sC_2r_{ds48}-1)}{r_{ds48}s(C_2+C_3)+1+\frac{r_{ds48}}{sL_2}-r_{ds48}g_{m48}}}{\frac{(1+r_{ds48}sC_2)(r_{ds48}g_{m48}-r_{ds48}sC_2-1)}{{r_{ds48}}^2s(C_2+C_3)+r_{ds48}+\frac{{r_{ds48}}^2}{sL_2}-{r_{ds48}}^2g_{m48}}-\left(s(C_2)+\frac{1}{r_{ds48}}+\frac{1}{sL_1}\right)}(26)$$

now we analyze the voltage gain A_V by inserting $r_{ds50}\approx\infty$.

$$A_V=\frac{g_{m48}+\frac{g_{m48}\left(g_{m48}-sC_2-\frac{1}{r_{ds48}}\right)}{s(C_2+C_3)+\frac{1}{r_{ds48}}+\frac{1}{sL_2}-g_{m48}}}{\frac{(\frac{1}{r_{ds48}}+sC_2)\left(g_{m48}-sC_2-\frac{1}{r_{ds48}}\right)}{s(C_2+C_3)+\frac{1}{r_{ds48}}+\frac{1}{sL_2}-g_{m48}}-\left(s(C_2)+\frac{1}{r_{ds48}}+\frac{1}{sL_1}\right)}(27.1)$$

$$A_V = \frac{g_{m48} + \frac{g_{m48}(g_{m48} - sC_2)}{s(C_2+C_3)+\frac{1}{sL_2}-g_{m48}}}{\frac{(sC_2)(g_{m48}-sC_2)}{s(C_2+C_3)+\frac{1}{sL_2}-g_{m48}} - s(C_2) - \frac{1}{sL_1}} \quad (27.2)$$

$$A_V = \frac{g_{m48}(s(C_2 + C_3) + \frac{1}{sL_2} - g_{m48}) + g_{m48}(g_{m48} - sC_2)}{(sC_2)(g_{m48} - sC_2) - (s(C_2 + C_3) + \frac{1}{sL_2} - g_{m48})(sC_2 + \frac{1}{sL_1})} \quad (27.3)$$

$$A_V = \frac{sg_{m48}(s^2(C_2 + C_3) + \frac{1}{L_2} - sg_{m48}) + sg_{m48}(g_{m48} - sC_2)}{(s^3C_2)(g_{m48} - sC_2) - (s^2(C_2 + C_3) + \frac{1}{L_2} - sg_{m48})(s^2C_2 + \frac{1}{L_1})} \quad (27.4)$$

Now by inserting $s = jw$ in Equation (27.4) and equating $A_V = 1$ we get

$$jwg_{m48}(-w^2(C_2 + C_3) + \frac{1}{L_2} - jwg_{m48}) + jwg_{m48}(g_{m48} - jwC_2) = -(jw^3C_2)(g_{m48} - jwC_2) - (-jw^2(C_2 + C_3) + \frac{1}{L_2} - jwg_{m48})(-jw^2C_2 + \frac{1}{L_1}) \quad (28)$$

$$-jwg_{m48}(C_2 + C_3) + \frac{jwg_{m48}}{L_2} + w^2{g_{m48}}^2 + {g_{m48}}^2 + w^2g_{m48}C_2 = -jw^3C_2g_{m48} - w^4{C_2}^2 + (w^2(C_2 + C_3) - \frac{1}{L_2} + jwg_{m48})\left(-jw^2C_2 + \frac{1}{L_1}\right) \quad (29)$$

$$-jwg_{m48}(C_2 + C_3) + \frac{jwg_{m48}}{L_2} + w^2{g_{m48}}^2 + {g_{m48}}^2 + w^2g_{m48}C_2 = -jw^3C_2g_{m48} - w^4{C_2}^2 - w^4C_2(C_2 + C_3) + \frac{w^2C_2}{L_2} - jw^3C_2g_{m48} + \frac{w(C_2+C_3)}{L_1} - \frac{1}{L_2L_1} + \frac{jwg_{m48}}{L_1} \quad (30)$$

$$w^4\left(2{C_2}^2 + C_2C_3\right) + w^3(-jg_{m48}(C_2 + C_3) + jC_2g_{m48} + jC_2g_{m48}) + w^2\left({g_{m48}}^2 + C_2g_{m48} - \frac{C_2}{L_2} - \frac{(C_2+C_3)}{L_1}\right) + w\left(\frac{jg_{m48}}{L_2} - \frac{jg_{m48}}{L_1}\right) + \left({g_{m48}}^2 - \frac{1}{L_2L_1}\right) = 0 \quad (31)$$

$$w^4\left(2{C_2}^2 + C_2C_3\right) + w^3(jg_{m48}(C_2 - C_3) + w^2\left({g_{m48}}^2 + C_2g_{m48} - \frac{C_2}{L_2} - \frac{C_2}{L_1} - \frac{C_3}{L_1}\right) + w\left(\frac{jg_{m48}}{L_2} - \frac{jg_{m48}}{L_1}\right) + \left({g_{m48}}^2 - \frac{1}{L_2L_1}\right) = 0 \quad (32)$$

On equating the imaginary part equal to zero from Equation (32) we get the expression of oscillation frequency.

$$w^3(g_{m48}(C_2 - C_3) + w\left(\frac{g_{m48}}{L_2} - \frac{g_{m48}}{L_1}\right) = 0$$

$$w^2(C_2 - C_3) = \left(\frac{L_1 - L_2}{L_2 L_1}\right)$$

$$w^2 = \left(\frac{L_1 - L_2}{L_2 L_1}\right)\left(\frac{1}{C_2 - C_3}\right)$$

$$w = \sqrt{\frac{(L_1 - L_2)}{L_2 L_1 (C_2 - C_3)}} \tag{33}$$

Publications

(1) Journal

Paper Title	Date	Journal Title
24GHz Frequency Synthesizer for Automotive Collision Avoidance Radar	Under review	International Journal of Electronics

(2) Conference

Paper Title	Date	Conference Title
A low power 12-bit 1MSps SAR ADC with capacitor array network	October 2016	2016 년도한국멀티미디어학회추계학술발표대회논문집제 19 권 2 호
An Ultra-Low Power 24GHz CMOS LC VCO	October 2016	2016 년도한국멀티미디어학회추계학술발표대회논문집제 19 권 2 호
Design of Digital FIR Filters for Noise Cancellation	October 2016	Proceedings of Conference on Information and Communication Engineering
Low-Power 24-GHz CMOS Low Noise Amplifier	October 2016	Proceedings of Conference on Information and Communication Engineering
Design of Phase Frequency Detector and Charge Pump for 24GHz PLL	June 2017	한국통신학회학술심포지움논문집

A Low-noise-Amplifier LNA 24 GHz CMOS Application	June 2017	한국통신학회학술심포지움논문집
Design Of Wide Bandwidth Low-Pass Filter for Phase-Locked Loop Applications	June 2017	한국통신학회학술심포지움논문집
Face Detection of Real-time Images using Feature-based Cascade Classifiers	June 2017	한국통신학회학술심포지움논문집
24GHz TSPC Frequency Divider for CMOS Application	December 2017	대한전자공학회학술심포지움논문집
Design of LNA for 24 GHz CMOS Application	December 2017	대한전자공학회학술심포지움논문집