



저작자표시-비영리-변경금지 2.0 대한민국

이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:



저작자표시. 귀하는 원저작자를 표시하여야 합니다.



비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.



변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 [이용허락규약\(Legal Code\)](#)을 이해하기 쉽게 요약한 것입니다.

[Disclaimer](#)

**Thesis for the Degree of Master of Engineering**

**Multiphysics Thermal Design of  
Packaged Power Terminals and Heater  
Plates for Wafer Thermal Processing**



**By**

**Dae Seong Woo**

**Department of Mechanical Design Engineering**

**The Graduate School**

**Pukyong National University**

**August 2018**

# **Multiphysics Thermal Design of Packaged Power Terminals and Heater Plates for Wafer Thermal Processing**

웨이퍼 열 공정에 사용되는 패키징된  
파워 단자부 및 히터 플레이트의  
다중물리적 열 설계

Advisor: Prof. Kyoung Joon Kim

by

Dae Seong Woo

A thesis submitted in partial fulfillment of the requirements  
for the degree of

Master of Engineering

in Department of Mechanical Design Engineering, the Graduate School  
Pukyong National University

**August 2018**

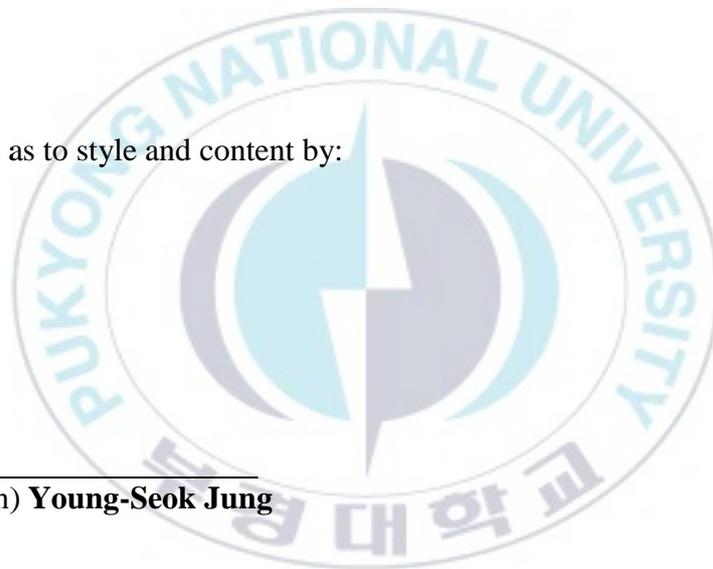
**Multiphysics Thermal Design of Packaged Power Terminals and  
Heater Plates for Wafer Thermal Processing**

A Thesis

by

Dae Seong Woo

Approved as to style and content by:



\_\_\_\_\_  
(Chairman) **Young-Seok Jung**

\_\_\_\_\_  
(Member) **Dong-In Yu**

\_\_\_\_\_  
(Member) **Kyoung Joon Kim**

August 24, 2018

## Acknowledgements

I would like to gratefully acknowledge the assistance and contribution of all people who helped me during my study.

First of all I would like to express my gratitude to my advisor and mentor Professor Kyoung Joon Kim for all advices, ideas, and supports that have been given such that I could finish all my research and thesis in Master program that I can be proud of. I really appreciate his knowledge and hard works that he has shown to me during my study in Thermal Management/Eco-Sustainability Laboratory (TME Lab).

I am very thankful to all members of TME Lab such as Byoung Guk, Nico Setiawan, Severianus Sony for their cooperation, kindness, and friendship that have been shown to me.

I am also really grateful to my close friends who have spent all kinds of the human emotions with me such as Jin Young, In Gu, Jae Beom, Jae Wook, Jin Woo, Min Ki.

Lastly, I would like to express my deepest gratitude to my father Young-Ok Woo, my mother Hyeong-Ja Cho, my younger brother Seung-Min Woo for their love, encouragement and support for me in the whole of my life.

Busan, 2018

Dae Seong Woo

# Contents

<b>Acknowledgment</b> .....	<b>i</b>
<b>Contents</b> .....	<b>ii</b>
<b>List of Figures</b> .....	<b>v</b>
<b>List of Tables</b> .....	<b>vii</b>
<b>Nomenclature</b> .....	<b>viii</b>
<b>Abstract</b> .....	<b>ix</b>
<b>I. Introduction</b> .....	<b>1</b>
1.1 Background and purpose .....	1
1.2 Objective and research method.....	2
1.3 Thesis outline.....	3
<b>II. FEA Modelling</b> .....	<b>4</b>
2.1 Packaged power terminals .....	4
2.1.1 Problem statment .....	5
2.1.2 Governing equation.....	6
2.1.3 Summary of aaumptions and material properties .....	6
2.1.4 FEA electrial-thermal model and boundary conditions .....	8
2.2 Heater plates .....	10
2.2.1 Problem statement.....	11
2.2.2 Governing equation.....	11
2.2.3 Summary of assumptions and material properties .....	12

2.2.4	FEA thermal model and boundary conditions .....	14
<b>III.</b>	<b>Experimental Methodology.....</b>	<b>17</b>
3.1	Experiment of PPT.....	17
3.1.1	Test rig design.....	17
3.1.2	Measurement equipment.....	19
3.1.3	Test procedure.....	21
3.1.4	Verification results.....	24
3.2	Experiment of HP .....	25
3.2.1	Test rig design.....	25
3.2.2	Measurement equipment.....	26
3.2.3	Test procedure.....	26
3.2.4	Verification results.....	27
<b>IV.</b>	<b>Results and Discussions.....</b>	<b>28</b>
4.1	Simulation results of PPT .....	28
4.1.1	Voltage and current density fields .....	29
4.1.2	Temperature fields .....	30
4.1.3	Boundary conditions effects .....	31
4.1.4	Substrate thickness effects .....	33
4.1.5	Encapsulant thermal conductivity effects .....	34
4.1.6	Heating element area effects.....	35
4.1.7	Solder contact area effects .....	37
4.1.8	Solder thickness effects .....	38

4.2	Simulation results of HP .....	40
4.2.1	Temperature fields .....	40
4.2.2	Heating element width effects .....	42
4.2.3	Zone and heating element gap effects.....	44
<b>V.</b>	<b>Conclusions.....</b>	<b>46</b>
	<b>List of Publications.....</b>	<b>48</b>
	<b>References .....</b>	<b>50</b>



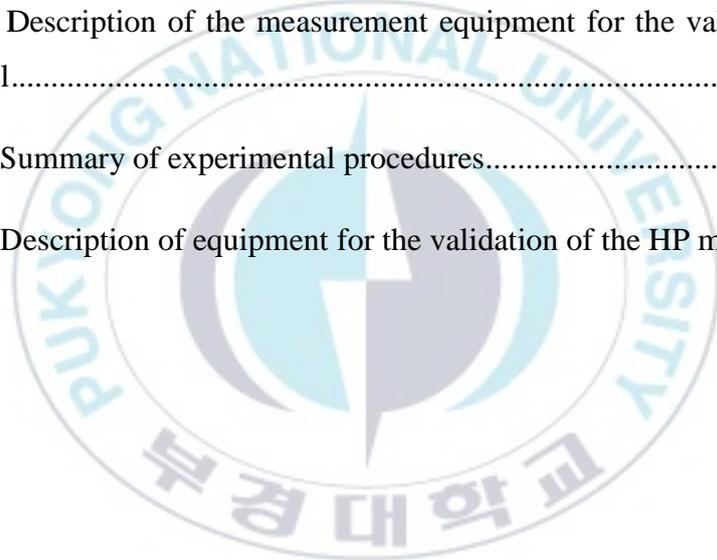
## List of Figures

Figure 2.1. (a) A heater plate and (b) the packaged power terminals of the bake unit. .....	5
Figure 2.2. The schematic of the structure and the material of a PPT.....	7
Figure 2.3. The FEA electrical-thermal model of a PPT.....	8
Figure 2.4. A heater plate of annealing unit .....	10
Figure 2.5. The schematic of 2-D and half-symmetry of the FEA thermal model...	12
Figure 2.6. The schematic of the structure and the material of a HP.....	13
Figure 2.7. The FEA thermal model of a HP .....	14
Figure 3.1. A test rig for the validation of the PT model.....	18
Figure 3.2. A test vehicle of a 1/8 arc HP.....	18
Figure 3.3. Experimental setup for the validation of the PPT model .....	20
Figure 3.4. The surface treated test vehicle .....	21
Figure 3.5. The measured temperature fields of the thermal images for each case..	23
Figure 3.6. Validation of the FEA electrical-thermal model .....	24
Figure 3.7. A test rig for the validation of the HP model .....	25
Figure 3.8. Validation of the FEA thermal model .....	27
Figure 4.1. The voltage fields of (a) the entire PPT and (b) the heating element.....	29
Figure 4.2. The current density fields of (a) the entire PPT and (b) the heating element .....	30

Figure 4.3. The temperature fields of (a) the entire PPT and (b) the heating element .....	31
Figure 4.4. The temperature fields for (a) the isothermal and (b) the effective heat transfer coefficient boundary conditions .....	32
Figure 4.5. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the substrate thickness.....	34
Figure 4.6. The maximum temperature of the heating element as a function of the encapsulant thermal conductivity .....	35
Figure 4.7. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the heating element area.....	36
Figure 4.8. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the solder contact area.....	38
Figure 4.9. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the solder thickness .....	39
Figure 4.10. The temperature field of the HP .....	40
Figure 4.11. (a) The average temperature and (b) the axial temperature of the upper surface of the HP .....	41
Figure 4.12. (a) The temperature fields of the HPs and (b) the axial temperature of the upper surface of the HPs as a function of the heating element width.....	43
Figure 4.13. (a) The schematics of each case and (b) the axial temperature of the upper surface of the HP as a function of the zone and the heating element gap .....	45

## List of Tables

Table 2.1 Summary of the PPT material properties .....	7
Table 2.2 Summary of numerical conditions of the PPT .....	9
Table 2.3 Summary of the HP material properties .....	13
Table 2.4 Summary of numerical conditions of the HP .....	16
Table 3.1 Description of a test vehicle .....	19
Table 3.2 Description of the measurement equipment for the validation of the PPT model.....	20
Table 3.3 Summary of experimental procedures.....	24
Table 3.4 Description of equipment for the validation of the HP model .....	26



## Nomenclature

$\rho_e$	Specific resistance ( $\Omega \cdot m$ )
$k$	Thermal conductivity Area ( $W/m \cdot K$ )
$q'''$	Volumetric rate of heat generation ( $W/m^3$ )
$\vec{J}$	Current density ( $A/m^2$ )
$\vec{E}$	Electric field ( $V/m$ )
$\alpha$	Coefficient of thermal expansion (ppm/K)
$V$	Voltage (V)
$h_{eff}$	Effective heat transfer coefficient ( $W/m^2 \cdot K$ )
$T$	Temperature ( $^{\circ}C$ )
$\rho$	Density ( $kg/m^3$ )
$C_p$	Specific heat (J/kg K)
$q''$	Heat flux ( $W/m^2$ )
$R$	Electrical resistance ( $\Omega$ )
$L$	Length (m)
$A$	Cross section ( $m^2$ )
$P$	Power (W)

# Multiphysics Thermal Design of Packaged Power Terminals and Heater Plates for Wafer Thermal Processing

Dae Seong Woo

Department of Mechanical Design Engineering, Graduate School,  
Pukyong National University

## Abstract

Heater plates (HPs) are main modules in the wafer thermal processing. The robustness of the HPs is critical to improve the reliability of the wafer thermal processing. However, failures of the packaged power terminals (PPTs) and the HPs frequently occur due to harsh thermal processing conditions. Therefore, thermal performances of the PPTs and the HPs should be carefully explored.

The finite element analysis (FEA) electrical-thermal model and the FEA thermal model were developed for the PPTs and the HPs, respectively, and verified by measurements. Various parametric influences on the thermal performance of the PPT were investigated by the FEA electrical-thermal models. In addition, the FEA thermal models explored influences of the heating element width, the gap between adjacent heating elements, and the heating zone gap on the thermal performances of the HPs including their effects on the axial temperature profiles of the upper surfaces of the HPs.

The study for PPTs has found a 10K higher temperature of the heating element compared with the substrate for the reference conditions of the PPTs. The parametric studies of the PPT show that the substrate thickness is a dominant parameter affecting the thermal performance of the PPT. It is seen that the axial temperature difference of the heating element decreases by 61% with the increase of the substrate thickness from 0.5mm to 5mm. The results show that associated with the increase of the heating

element area, the solder contact area, and the solder thickness, the value of the maximum temperature of the heating element is slightly reduced by nearly 1%. However, it is seen that the value of the axial temperature difference of heating element is substantially reduced by about 10%. The parametric study for the HPs has found that the effect of the heating element width on the heater performance is negligible. The optimum design of the heating zone and the heating element gap could considerably alleviate the axial temperature difference of the upper surface of the HP by 56% compared with the baseline condition.



# I. Introduction

## 1.1 Background and purpose

Heater plates (HPs) of the bake and the annealing unit in the spinner, which are semiconductor manufacturing equipment, are the core modules of the wafer thermal processing [1, 2]. The HPs used in the baking processing affects time reduction of the dehydration bake, pre bake, and post bake [3-6]. In addition, annealing uses a high-temperature oxidation processing to reduce structural defects in the silicon, stress, and interface charge [7, 8]. The HPs used at this time have an immense influence on the annealing processing. In general, the HPs are sophisticated thermal processing modules requiring a temperature tolerance within 2°C. Therefore, research to ensure temperature uniformity of the HPs is essential [3-6, 9-15]. Most studies have been carried out to maintain a uniform temperature of the HPs using the controller, while several studies have been conducted to reduce the temperature gradient [5-8, 11, 16]. Zhang et al [10] developed the new PEB thermal modules design together with a novel robust control methodology that led the uniformity in steady-state condition. Jinho Lee et al [3] designed a new heater pattern for 300mm wafer to reduce the temperature non-uniformity. Nevertheless, failures often occur during the wafer thermal processing because of the temperature gradient in the HPs.

The main factor of the temperature gradient generated in the HPs is due to the harsh thermal processing conditions caused by complicated heating elements, high heat density of heating elements, and dynamic temperature controls [6, 9, 12-14]. Therefore, this study aims to understand the thermal background of the HPs based on the precise thermal design to improve the reliability of the wafer thermal processing. In addition, this study conducts research to physically alleviate the temperature-oriented failure by simplifying the complicated structure of heating elements.

On the other hand, harsh thermal processing conditions frequently cause thermal failures in the PPTs of HPs. It has a profound influence on the failure of HPs. However, researches on the PPT are very insufficient, unlike research to obtain temperature uniformity of the HPs. Therefore, this study aims to understand the thermal-background of the PPTs failure and to investigate the thermal performance of the PPTs by conducting sophisticated multi-physical analysis.

## **1.2 Objective and research method**

The objective of this thesis is to present a combined numerical and experimental method to investigate the thermal performances of the PPT and the HP, which have a profound impact on the failure factors during thermal processing in the bake and the annealing unit. The results of this study are expected to have a significant effect on the reliability of the wafer thermal processing. To accomplish this, the followings are done.

First, this thesis discusses the finite element analysis (FEA) electrical-thermal model of the PPT and the FEA thermal model of the HP developed by utilizing ANSYS Multiphysics [17]. The assumptions, material properties, and boundary conditions of each model are presented.

Second, the thesis shows the verifications of the FEA electrical-thermal model and FEA thermal model by comparing predictions of each model with measurements. In addition, the test rig, measurement equipment, and test procedure of the PPT and the HP are presented.

Finally, the thesis discusses numerically-analyzed thermal performances of PPT and HP associated with various parametric effects.

### **1.3 Thesis outline**

This section briefly describes the contents of the thesis. The contents consist of five parts, i.e. introduction, FEA modelling, experimental study, results and discussions, and conclusions as follow:

#### **Chapter 1: Introduction**

In this chapter, the background and purpose of this thesis are described. The objective and research method of this thesis are then presented. Finally, the outline of this thesis are explained.

#### **Chapter 2: FEA modeling**

This chapter describes the numerical methodology used to predict the thermal performances of the PPT and the HP. The physical structures of the PPT and HP are explained. The problem statement, governing equation, assumption, and material properties for each model are outlined. The FEA models of the PPT and the HP and their boundary conditions are shown to make sure the models are accurate.

#### **Chapter 3: Experimental methodology**

This chapter describes the designs and applications of the test rig. The measurement equipment and test procedure are detailed. The validation results for the measurements are shown.

#### **Chapter 4: Results and discussion**

This chapter shows the simulation results, i.e. the voltage, the current density, the temperature fields and the effects of boundary conditions, the substrate thickness, the encapsulant thermal conductivity, the heating element area, the solder contact area, and the solder thickness of the PPT. The temperature fields, the heating element width effects, the zone and the heating element gap effects of the HP are also described.

#### **Chapter 5: Conclusions**

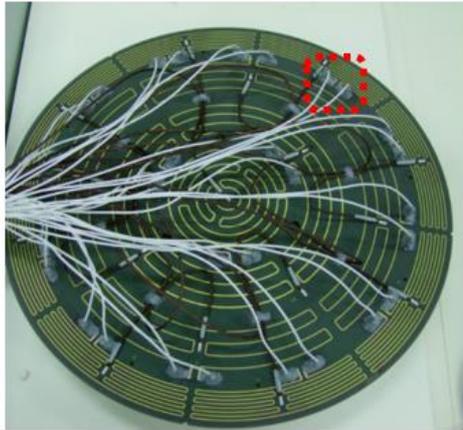
Conclusions from this research and expected effect are presented.

## II. FEA modelling

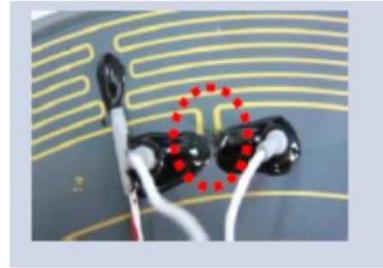
The objectives of the FEA modelling are to get the predicted data of the thermal performances of the PPT and the HP and to propose solutions to the failure factors that occur in each case. To accomplish this objective, the followings are done. The physical structures of the PPTs and HPs are pictured in sections 2.1 and 2.2 respectively. In the following paragraphs, the problem statement, governing equations, assumption, and material properties for each model are outlined. Then, the FEA model and boundary conditions of the PPT and the HP are shown, and the methodologies for the simulation are described.

### 2.1 Packaged power terminals

Figure 2.1 shows an actual picture of a HP and the PPTs of the bake unit. Figure 2.1 (a) is actual image of a HP, and figure 2.1 (b) shows an enlarged image of the dotted line in figure 2.1 (a). The dotted line of figure 2.1 (b) indicates a pair of the PPTs, and shows surrounding heating elements. The radius and thickness of the HP are 157mm and 3.4mm. The width of the heating element is shown in figure 2.1, which shows the difference between the zones. This study investigates outlying zones where failures often occur, with 0.7mm heating element width.



(a)



(b)

**Figure 2.1. (a) A heater plate and (b) the packaged power terminals of the bake unit.**

### 2.1.1 Problem statement

Failures of the components related to temperature account for about 80% in bake unit and over 90% of failures of components related to temperature occur in the PPTs. The failure is caused by thermal problems in the PPTs, causing damage to the heating element, resulting in failure in the bake unit. However, failures consistently occur in the PPTs without known cause of the thermal problem in the PPTs. Therefore, understanding and improving the cause of thermal problems in the PPTs is expected to improve the reliability of the bake unit.

### 2.1.2 Governing equation

A fully-coupled FEA electrical-thermal model is required to numerically investigate the thermal performance of the PPT. The governing equations for a steady state heat transfer of FEA model are shown in equations 1 to 3 [17, 18].

Voltage distribution equation is written as

$$\nabla \cdot \frac{\nabla \phi}{\rho_e} = 0 \quad (1)$$

Heat conduction equation is written as

$$\nabla \cdot (k\nabla T) + q''' = 0 \quad (2)$$

In the model,  $q'''$  results from joule heating and is written as

$$q''' = \vec{j} \cdot \vec{E} \quad (3)$$

Where,  $\phi$  is the voltage distribution,  $\rho_e$  is the specific resistance,  $k$  is the thermal conductivity,  $T$  is the temperature,  $q'''$  is the volumetric rate of heat generation,  $\vec{j}$  is the current density, and  $\vec{E}$  is the electric field.

### 2.1.3 Summary of assumptions and material properties

This sub-section outline the assumptions and material properties used to model the thermal and electrical flows in the PPT numerical analysis, summarized as follows.

- Steady state
- Two dimensional
- Heat conduction
- Top and both sides insulated

Figure 2.2 shows the schematic of the structure and material of the PPT. The substrate, the heating element, the solder, and the power terminal are composed of AlN, NiP(8%P), SnSb(5%Sb) and Cu, respectively. The primary material properties used in the FEA electrical-thermal model are summarized in table 2.1.

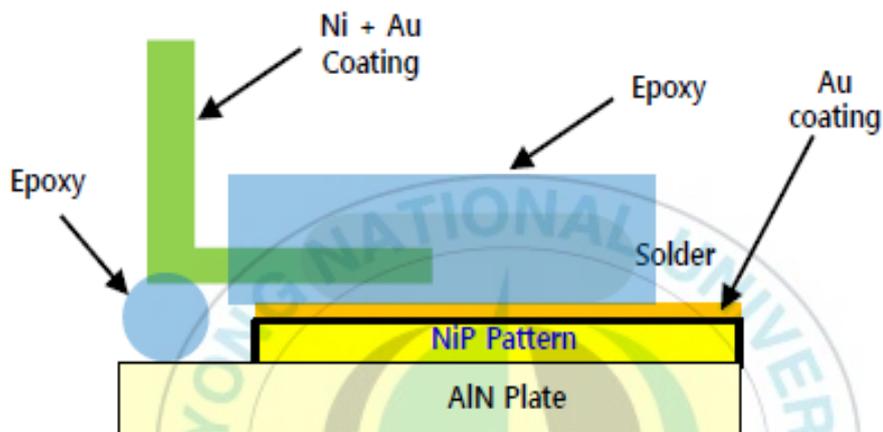


Figure 2.2. The schematic of the structure and the material of a PPT

Table 2.1 Summary of the PPT material properties

	Material	Thermal conductivity	CTE
HP(Substrate)	AlN	170 W/m-K	5 ppm/K
Heating element	NiP(8%P)	91 W/m-K	13 ppm/K
Solder	SnSb(5%Sb)	55 W/m-K	23 ppm/K
Power terminal	Cu	390 W/m-K	17 ppm/K
Epoxy	Epoxy resin	0.2 W/m-K	50 ppm/K

### 2.1.4 FEA electrical-thermal model and boundary conditions

This sub-section describes the 2-D FEA electrical-thermal model and boundary conditions developed by utilizing a commercial software, ANSYS Multiphysics, to investigate the temperature fields and thermal performance of the PPT. The FEA electrical-thermal model of the PPT is modeled from the bottom surface to the upper surface in the following order; substrate, heating element, solder, power terminal, and epoxy. The structure of the model is shown in figure 2.3. The dimensions of the entire and heating element of the FEA electrical-thermal model are 15.8mm x 7mm and 7.56mm x 0.03mm. 182k quadrilateral computational elements are used.

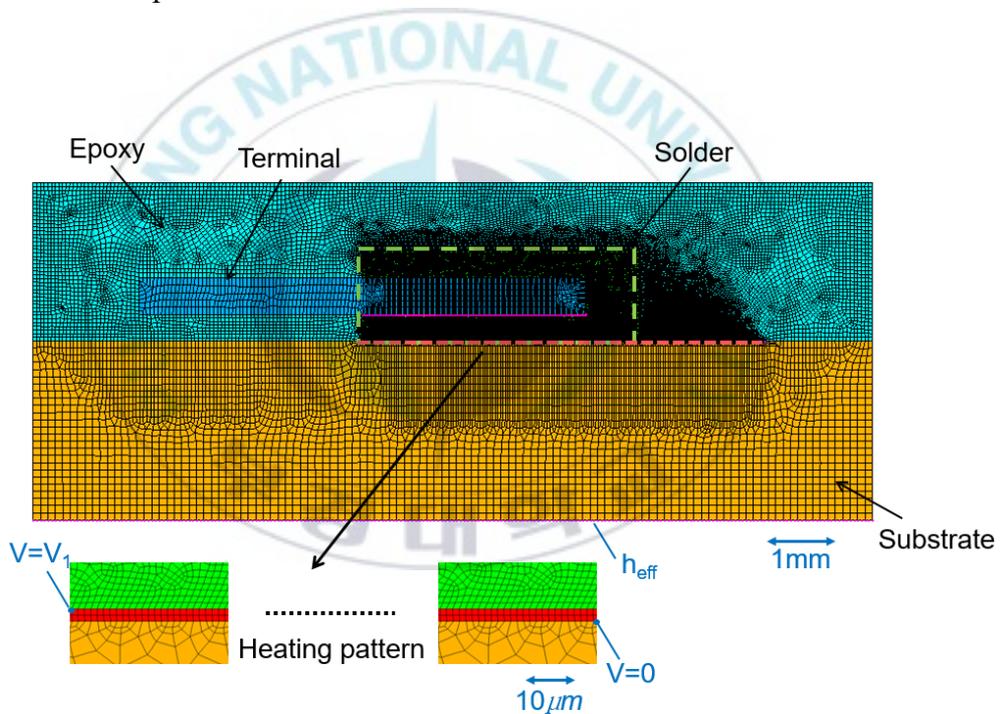


Figure 2.3. The FEA electrical-thermal model of a PPT

The electrical load and thermal boundary conditions of the electrical-thermal model are shown in figure 2.3. Where  $h_{eff}$  and  $V_1$  are the effective heat transfer coefficient and DC voltage, respectively.  $V_1$  was obtained by considering the resistance of heating element in the model and calculated the using ohm's law with the actually applied current.  $h_{eff}$  was defined by considering the heat rate in the PPT to which the voltage of 3V was applied and iterative calculation was numerically performed until the average temperature on the lower surface of the substrate converged to the processing temperature of 110°C to determine  $h_{eff}$ . In this study,  $h_{eff}$  is determined to 3540W/m<sup>2</sup> · K, and  $V_1$  is determined to 3V. The representative numerical conditions for the FEA electrical-thermal model are summarized in table 2.2.

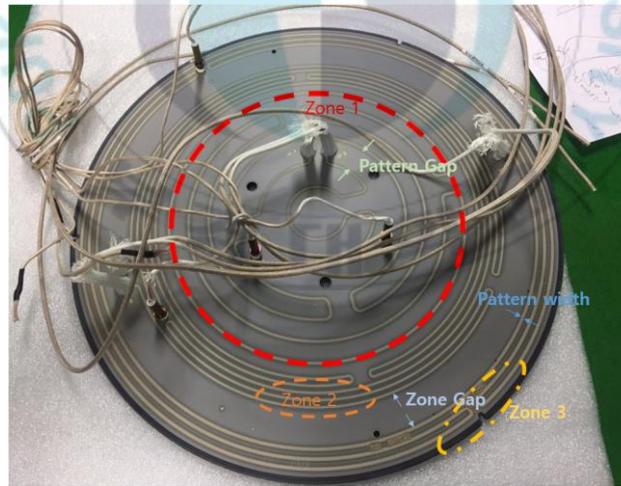
The processes of multiphysical simulation in the FEA electrical-thermal model of the PPT are as follows. The DC Voltage is applied to the heating element, the current flows, the heat is generated by ohmic loss, the generated heat diffuses by thermal conduction, and finally dissipated from the lower surface of the substrate to the outside.

**Table 2.2 Summary of numerical conditions of the PPT**

<i>Physical conditions</i>	
FEA model dimension	15.8mm x 7mm
Heating element dimension	7.56mm x 0.03mm
<i>Electrical and thermal conditions</i>	
Applied voltage	3V DC
Effective heat transfer coefficient	3540W/m <sup>2</sup> · K
<i>Computational element</i>	
Number of element	182 x 10 <sup>3</sup>
Type of element	quadrilateral
<i>Solution model</i>	
State	Steady state
Multiphysics model	Electrical-thermal model

## 2.2 Heater plates

HPs are a sophisticated thermal processing module that has a profound effect on the wafer thermal processing. An actual image of a HP in the annealing unit is shown in figure 2.4. Figure 2.4 is the HP used at high temperature of 400°C. The HP is divided into zone 1~ zone 3 according to the area of the heating element, and dynamic temperature control is being performed to maintain processing temperature. Dynamic temperature controls are actually applied to each zone through the zero-crossing control method, but in this study, the same energies of applied power to each zone are applied as the unsteady heat flux. An external diameter and thickness of the HP are 330mm and 4mm. As shown in figure 2.4, the widths of the heating elements are 1.4mm, 1.2mm, and 1.8mm in zone 1 ~ zone 3, respectively. The gaps of the heating elements and the zones are also different.



**Figure 2.4. A heater plate of annealing unit**

### 2.2.1 Problem statement

The problem of temperature uniformity of the HP in the wafer thermal processing has been studied steadily. Most studies have attempted to maintain the temperature uniformity of the HP through the control method. However, the temperature uniformity problems are still happening. Therefore, the thermal performance of the HP should be investigated. Because the temperature gradient in the HP is caused by the robust thermal processing due to the complicated structure of heating elements, high heat density of heating elements etc. This study is conducted to alleviate the failure factors, by simplifying the complicated structure of heating elements based on the precise thermal design.

### 2.2.2 Governing equation

The FEA thermal model is required in order to numerically investigate the thermal performance of HP, and the governing equations for a transient state heat transfer of the FEA model are shown in equation 4 below [17, 18].

Heat conduction equation is written as

$$\nabla \cdot (k\nabla T) + q''' = \rho c \frac{\partial T}{\partial t} \quad (4)$$

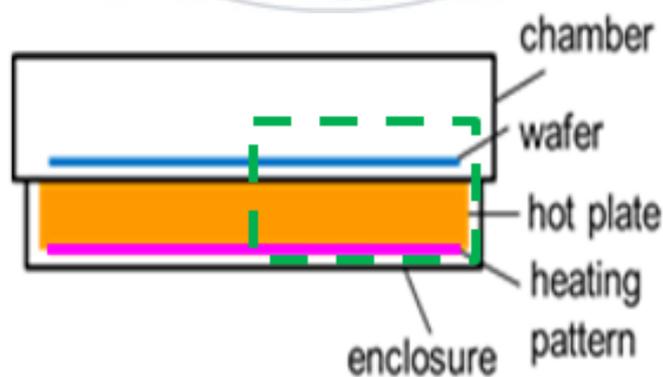
Where, k is the thermal conductivity, T is the temperature, and  $q'''$  is the volumetric rate of heat generation.

### 2.2.3 Summary of assumptions and material properties

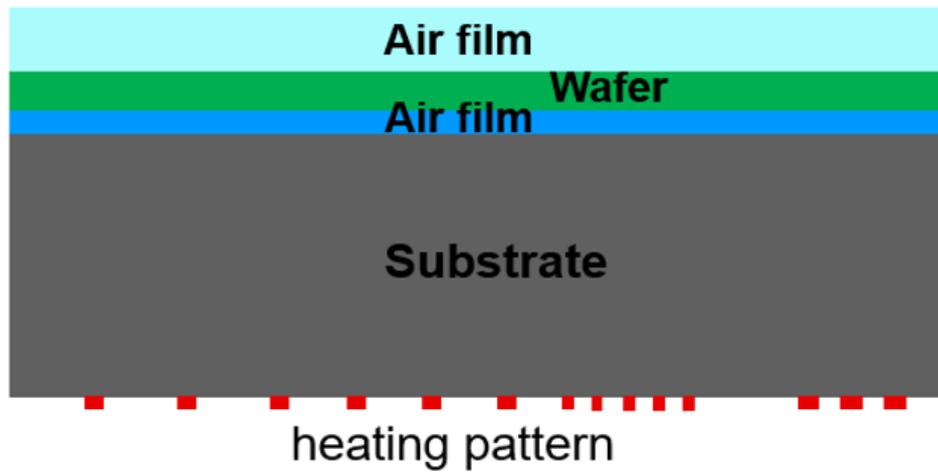
This sub-section outlines the assumptions and material properties of the FEA thermal model in the HP numerical analysis, summarized as follows.

- Transient state
- Two dimensional
- Half-symmetry
- Heat conduction
- Both sides insulated

The entire schematic of the 2-D and half-symmetry of the FEA thermal model is shown in figure 2.5. Figure 2.6 shows the schematic of the structure and material properties of the HP model, which is upside-down of figure 2.4. The substrate, the air film, and the wafer are composed of AlN, Air, and Si, respectively. The primary material properties used in the FEA thermal model are summarized in table 2.3.



**Figure 2.5. The schematic of 2-D and half-symmetry of the FEA thermal model**



**Figure 2.6. The schematic of the structure and the material of a HP**

**Table 2.3 Summary of the HP material properties**

	Material	Thermal conductivity	Density	Specific heat
HP(Substrate)	AlN	170 W/m-K	3300 kg/m <sup>3</sup>	740 J/kg-K
Air film	Air	0.026 W/m-K	1.16 kg/m <sup>3</sup>	1007 J/kg-K
Wafer	Si	124 W/m-K	2329 kg/m <sup>3</sup>	794 J/kg-K

### 2.2.4 FEA thermal model and boundary conditions

This sub-section describes the 2-D FEA thermal model and boundary conditions developed by utilizing a commercial software, ANSYS Multiphysics, to investigate the temperature fields and thermal performances of the HPs. The FEA thermal model of the HP is modeled in the order of heating element, substrate, air film, wafer, and air film from the bottom, and the structure is shown in figure 2.7. The entire dimension of the FEA thermal model is 165mm x 6mm, and approximately 43k quadrilateral computational elements are used. Also, the thickness of substrate, air film, wafer, and air film are 4mm, 0.3mm, 0.7mm, and 1mm, respectively. The widths of heating elements of the each zone are 1.4mm, 1.2mm, and 1.8mm, respectively.

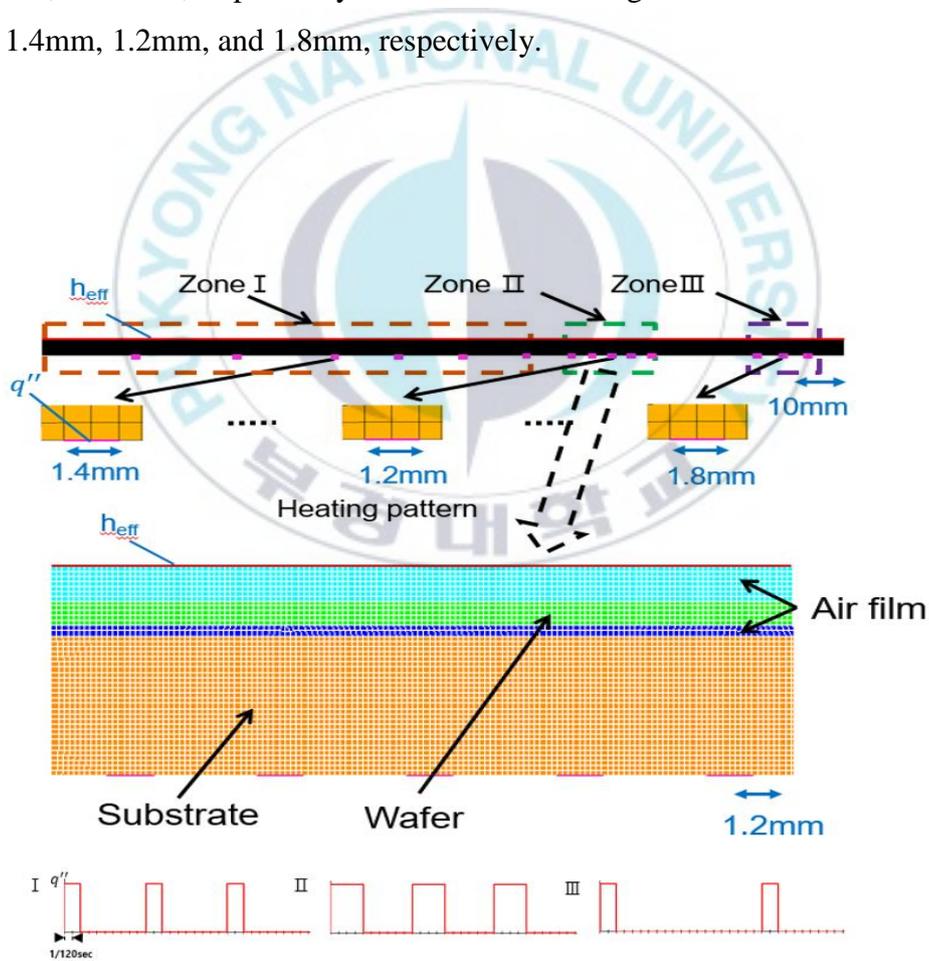


Figure 2.7. The FEA thermal model of a HP

The thermal boundary conditions of the FEA thermal model are shown in figure 2.7. Where  $h_{eff}$  is the effective heat transfer coefficient and  $q''$  is the heat flux. In this study,  $q''$  were obtained by dividing the applied power to each zone by the heating element area of each zone.  $h_{eff}$  is determined by finding the energy equilibrium considering the applied heat rate to the heating element of the HP and iterative calculation was numerically performed until the average temperature of the upper surface of the substrate converged to the processing temperature of 400°C to obtain  $h_{eff}$ .  $q''$  are determined to  $365 \times 10^3 \text{ W/m}^2$ ,  $158 \times 10^3 \text{ W/m}^2$ , and  $237 \times 10^3 \text{ W/m}^2$  for each zone, and  $h_{eff}$  is determined to  $365 \text{ W/m}^2 \cdot \text{K}$ . The representative numerical conditions for the FEA thermal model are summarized in table 2.4.

The processes of simulation in the FEA thermal model of the HP are as follows. The heat flux is applied dynamically to the heating element, and diffused in the order of the substrate, the air film, the wafer, and the air film by heat conduction and finally dissipated from the upper surface of the air film to the outside.

**Table 2.4 Summary of numerical conditions of the HP**

<i>Physical conditions</i>	
FEA model dimension	165mm x 6mm
HP thickness	4mm
Air film	0.3mm
Wafer thickness	0.7mm
Air film	1mm
<i>Boundary and thermal conditions</i>	
Heat flux in the heating elements	I: $365 \times 10^3 \text{ W/m}^2$
	II: $158 \times 10^3 \text{ W/m}^2$
	III: $237 \times 10^3 \text{ W/m}^2$
Effective heat transfer coefficient	$365 \text{ W/m}^2 \cdot \text{K}$
<i>Computational element</i>	
Number of element	$43 \times 10^3$
Type of element	Quadrilateral
<i>Solution model</i>	
State	Transient-state
Coordinate system	Half-axial symmetry
Multiphysics model	Thermal model

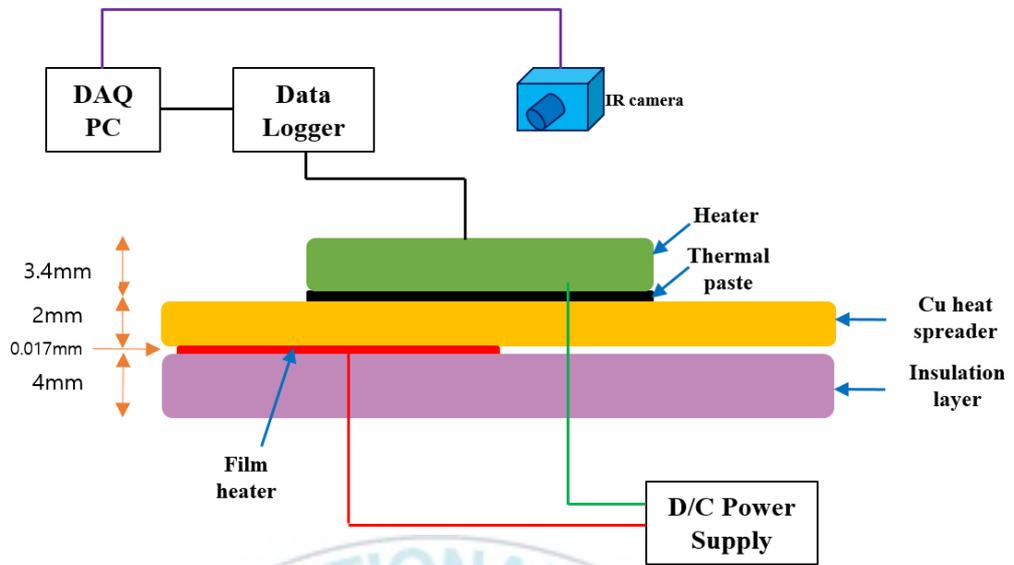
### **III. Experimental Methodology**

The purpose of the experimental study is to check the validity of the numerical prediction. The investigations of the PPT and the HP were conducted for each case. In this chapter, the test rig, and the measurement equipment were prepared. The test procedure and the validation results of the measurements are explained in the following section. For the PPT, the experiment was tested by using a 1/8 arc HP with a radius of 157mm. For the case of the HP, the experiment was tested while maintaining the processing temperature through dynamic temperature control.

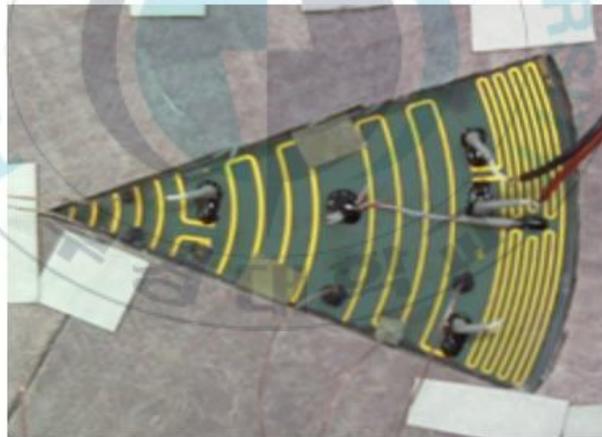
#### **3.1 Experiment of PPT**

##### **3.1.1 Test rig design**

A test rig of the HP for the verification purpose of the FEA electrical-thermal model of the PPT has been designed, as shown in figure 3.1. A test vehicle was composed of a HP, a heat spreader, a film heater, and the insulation layer. A test vehicle was a 1/8 arc HP with a radius of 157mm and the actual image is shown in figure 3.2. A copper plate of high thermal conductivity was used as a heat spreader. A 127mm x 127mm polyimide heater was attached to the bottom of a heater spreader to match the experimental environment. Lastly, aerogel insulation was used in the insulation layer to prevent heat loss. The components of a test vehicle are summarized in table 3.1.



**Figure 3.1. A test rig for the validation of the PPT model**



**Figure 3.2. A test vehicle of a 1/8 arc HP**

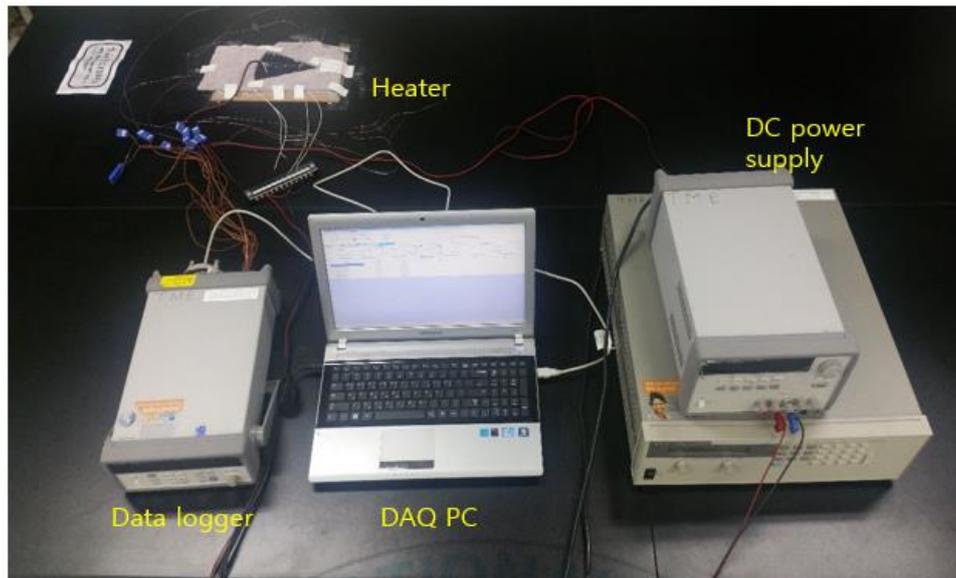
**Table 3.1 Description of a test vehicle**

Components	
Heater plate	1/8 Arc heater plate (Radius : 157mm)
Heat spreader	Copper (150mm x 270mm)
Film heater	Polyimide heater (127mm x 127mm)
Insulation layer	Aerogel insulation

### **3.1.2 Measurement equipment**

Figure 3.4 displays the measurement equipment and the test rig. The measurement equipment were composed of an infrared camera, a data logger, the DC power supply, and a DAQ PC. Information on the measurement equipment are summarized in table 3.2.

An Agilent 6655A and an Agilent E3634A DC power supply were utilized to provide electric power to the HP and to a film heater, respectively. An Agilent 34970A data logger was deployed to obtain the temperature reading. A DAQ PC was used to monitor and store the temperature data from the data logger.



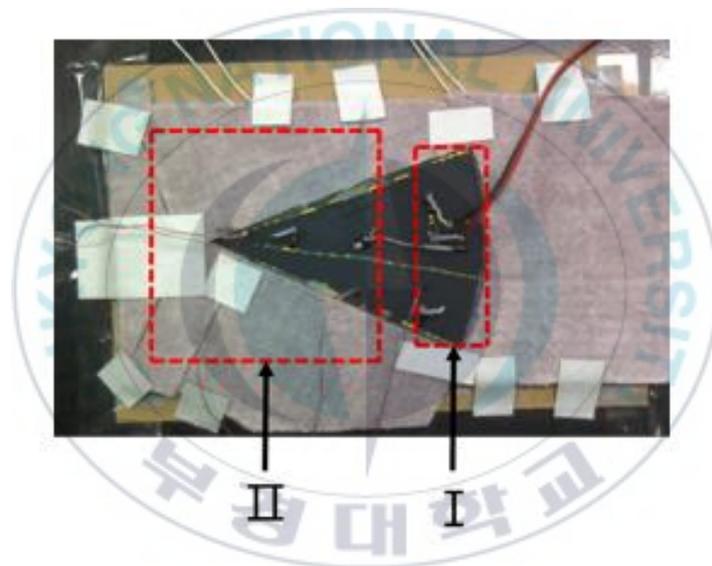
**Figure 3.3. Experimental setup for the validation of the PPT model**

**Table 3.2 Description of the measurement equipment for the validation of the PPT model**

Equipment	
Infrared camera	FLIR T440
DC power supply	Agilent 6655A, Agilent E3634A
Data logger	Agilent 3490A
DAQ PC	Notebook PC

### 3.1.3 Test procedure

The numerically predicted values of the epoxy surface temperature, which is the encapsulant of the PPT, have been compared with the measured temperatures in order to verify the validity of the model. An infrared camera was used for temperature measurement. The surface of the HP was coated with black paint in order to consider the measurement error caused by the thermal radiation of the epoxy surface at the time of measurement. Effective emissivity was set to 0.95 when acquiring the thermal images. The surface treated HP is shown in figure 3.4.



**Figure 3.4. The surface treated test vehicle**

The experiment was tested in three cases a, b, and c. Part II in the figure 3.4 was the film heater, and the film heater was used to maintain temperature of the lower surface of the substrate uniformly. Part I was the applied power to the HP, and the currents were applied at 0.282A, 0.415A, and 0.513A for each case. The measured data are the average temperatures of the epoxy surfaces for each case, and the thermal images for cases a to c is shown in figure 3.5. The numerical data are also the average temperatures of the epoxy surfaces for each

case. In the numerical values, the applied current to the part I in each case were applied as the values of the replacement DC voltage in the FEA electrical-thermal model. The applied voltages in each case are 0.761V, 1.121V and 1.385V, respectively. The experimental procedures are summarized in table 3.3.

The equations used for replacement are shown in equation (5) and (6) below [19].

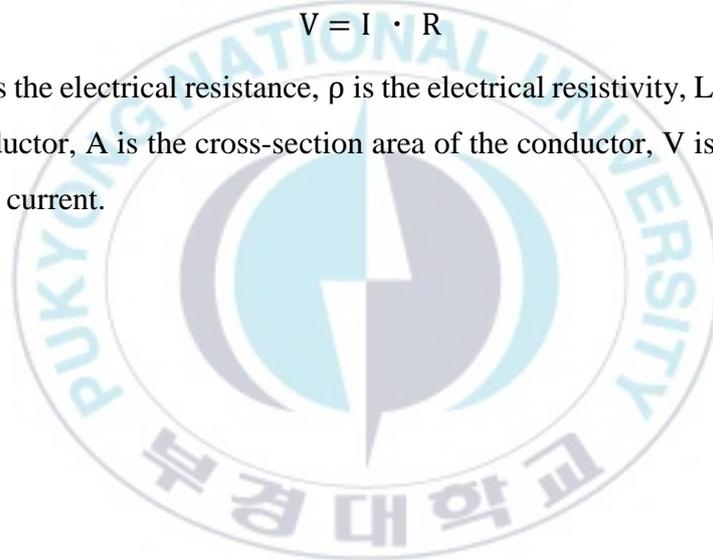
Electrical resistance equation is written as

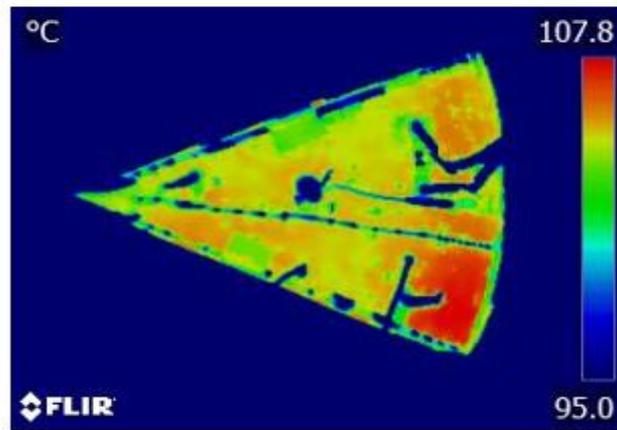
$$R = \rho \frac{L}{A} \quad (5)$$

Ohm's law equation is written as

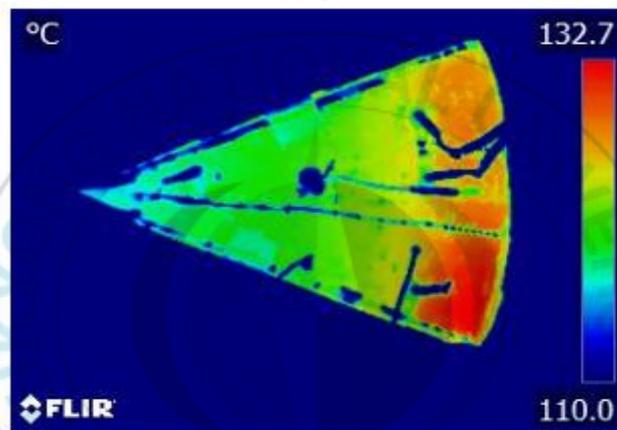
$$V = I \cdot R \quad (6)$$

Where, R is the electrical resistance,  $\rho$  is the electrical resistivity, L is the length of the conductor, A is the cross-section area of the conductor, V is the voltage, and I is the current.

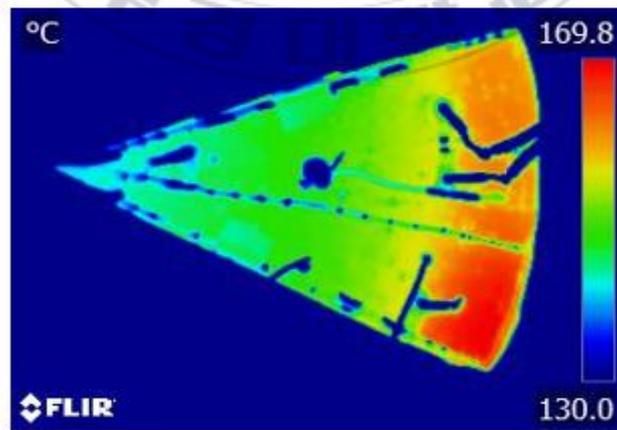




(a)



(b)



(c)

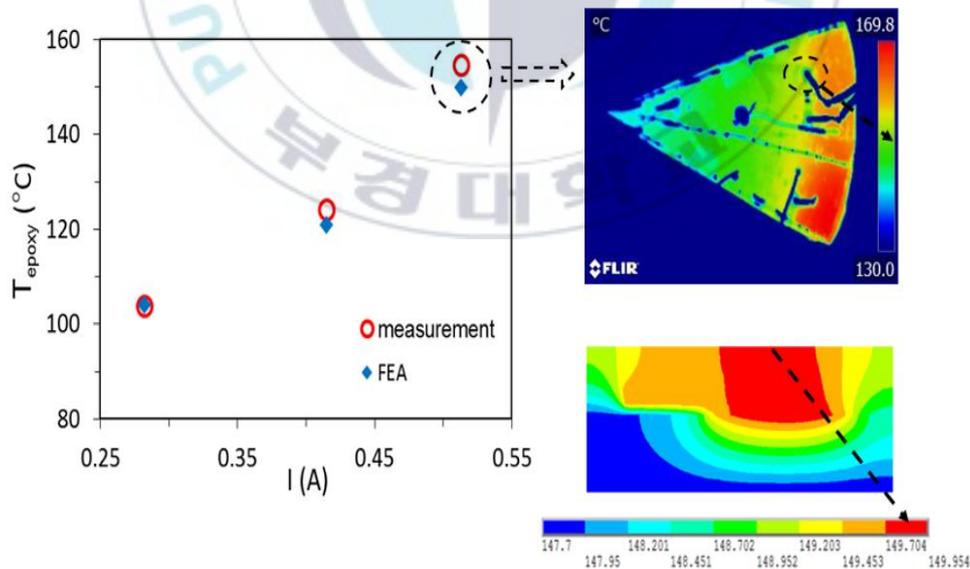
Figure 3.5. The measured temperature fields of the thermal images for each case

**Table 3.3 Summary of experimental procedures**

Case	Measurement			FEA	
	Power I(W)	Power II(W)	Current (A)	Voltage (V)	$T_s$ (°C)
a	16	20	0.282	0.761	103.4
b	35	10	0.415	1.121	119.5
c	55	10	0.513	1.385	147.7

### 3.1.4 Verification results

To validate the FEA electrical-thermal model, the measured temperatures of the epoxy surface were compared with the numerically predicted values by the model. The results are shown in figure 3.6. The validity of the FEA electrical-thermal model was verified with the maximum discrepancy of 3% between the measured and numerical data. Therefore, the FEA electrical-thermal model can be used effectively as an analytical model.



**Figure 3.6. Validation of the FEA electrical-thermal model**

## 3.2 Experiment of HP

### 3.2.1 Test rig design

A test rig for the verification purpose of the FEA thermal model of the HP has been designed, as shown in figure 3.7. In this experiment, a test vehicle of a HP with an external diameter of 330mm and a thickness of 4mm was used. The air flow from the outside to the HP was blocked by an enclosure. The support fixtures were located in the center of the HP to support the HP, as shown in figure 2.4 and figure 3.7. This study was conducted to investigate the temperature uniformity of the HP. Therefore, the experiment was tested without the wafer in order to measure the temperature of the upper surface of the HP through the infrared camera.

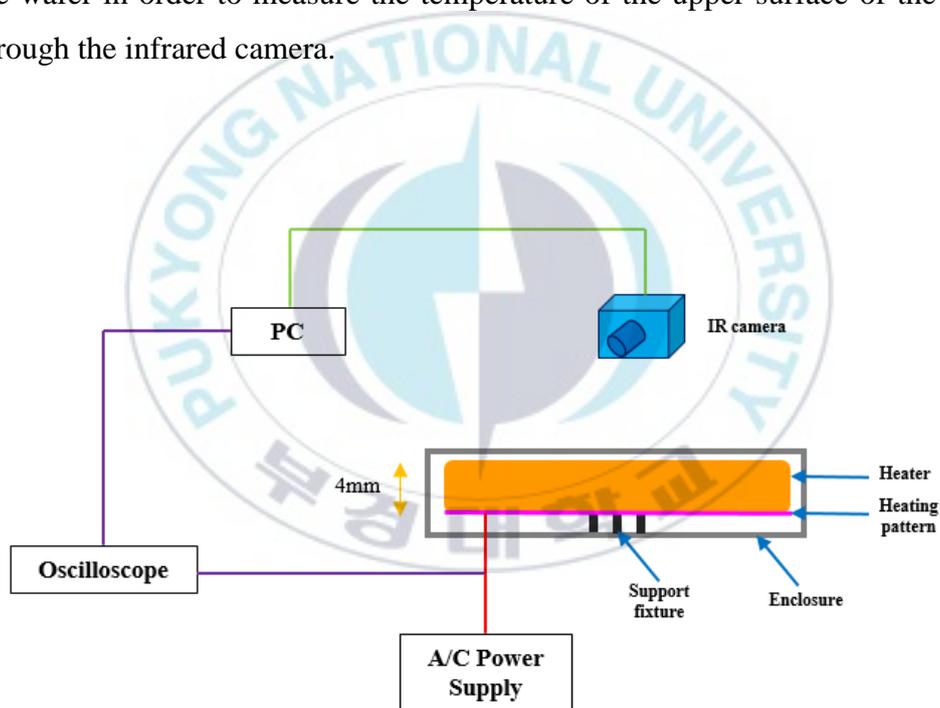


Figure 3.7. A test rig for the validation of the HP model

### 3.2.2 Measurement equipment

The measurement equipment were composed of an infrared camera, an oscilloscope, an AC power supply, and a PC. Information on the measurement equipment are summarized in table 3.4.

The measurement temperatures were obtained utilizing an infrared camera, FLIR T440. An Agilent AC6804A AC power supply was used to provide electrical power to the HP. The DSOX3014T oscilloscope was deployed to obtain the applied voltage for the time. Lastly, a PC was used to monitor the temperature and the voltage data.

**Table 3.4 Description of equipment for the validation of the HP model**

Equipment	
Infrared camera	FLIR T440
Oscilloscope	DSOX3014T
AC power supply	Agilent AC6804A
PC	Notebook PC

### 3.2.3 Test procedure

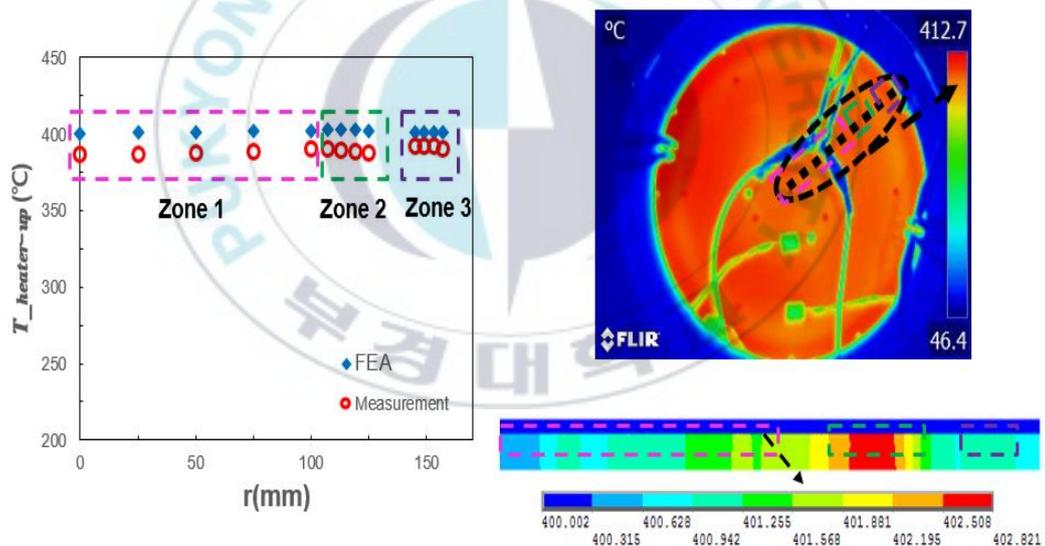
The numerically predicted values of the axial temperatures of the upper surface of the HP have been compared with the measured temperatures in order to verify the validity of the model. An infrared camera was used for temperature measurement. The effective emissivity was set to 0.95 when acquiring the thermal images due to the black surface of the HP.

The experiment was conducted when the temperature of the upper surface of the HP was steady state by applying voltage of 20%, 40%, and 10% to zone 1 ~ zone 3, respectively. The measured data were the axial average temperatures of the upper surface of the HP in the thermal image acquired from repeated experiments for a period of time when the temperature was steady state. The load conditions of the numerical values were replaced by the heat flux equal in energy to the applied power to each zone. The numerical data were the axial

temperatures of the upper surface of the HP at the same position as the measured data.

### 3.2.4 Verification results

To validate the FEA thermal model, the measured temperatures of the axial direction of the upper surface of the HP were compared with the numerically predicted values by the FEA model under the dynamic load conditions. The results are shown in figure 3.8. The validity of the FEA thermal model was verified with the maximum discrepancy of 3.7% between the measured and numerical data. Therefore, the FEA thermal model can be used effectively as an analytical model.



**Figure 3.8. Validation of the FEA thermal model**

## IV. Results and Discussions

This chapter describes the simulation results in detail using the verified models of the PPT and the HP. The simulation results of the PPT discuss the voltage field, the current density field, the temperature field, and the parametric effects. The parametric studies of the PPT involve the effects of the boundary conditions, the substrate thickness, the thermal conductivity of the encapsulant, and so on. In the next section, the simulation results of the HP discuss the temperature field and the parametric effects. The parametric studies of the HP include the effects of the heating element width, the zone and the heating element gap.

### 4.1 Simulation results of PPT

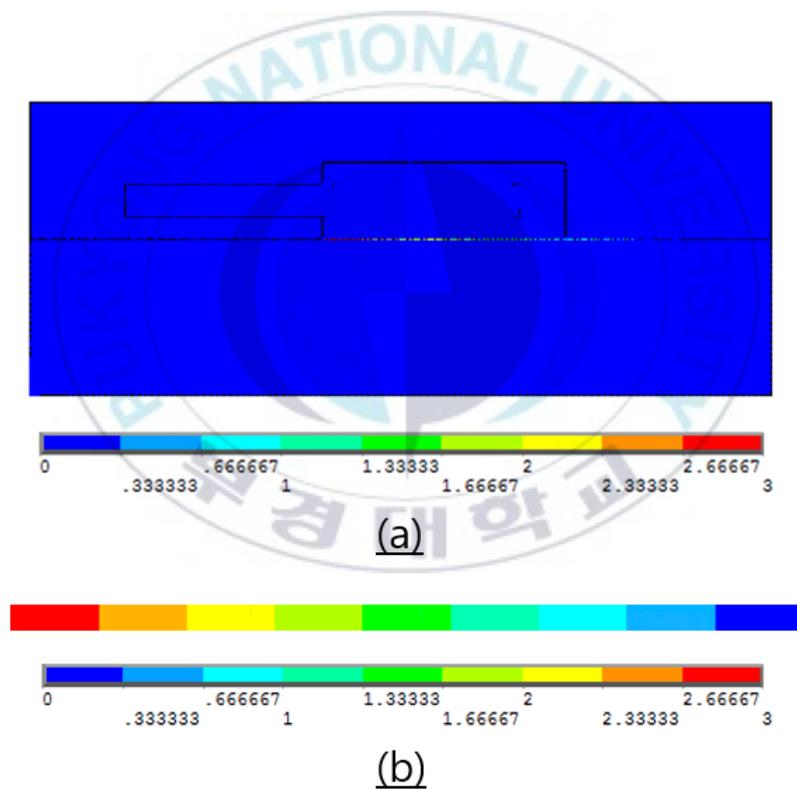
This section discusses the thermal performances of the PPT using the FEA electrical-thermal model to apply the electrical load and the actual load conditions to the PPT model. The results of the analysis show the voltage field, the current density field, and temperature field of the PPT. This section also discusses the results of the boundary conditions, the substrate thickness, the encapsulant thermal conductivity, the heating element area, the solder contact area, and the solder thickness effects on the thermal performances of the PPT.

When calculating the numerical results, the representative dimensions of the FEA electrical-thermal model are as follows. A substrate thickness is 3.4mm, an encapsulant thermal conductivity is 0.2W/m-K, a heating element length is 4.2mm, a solder length is 5.2mm, and a solder thickness is 0.5mm.

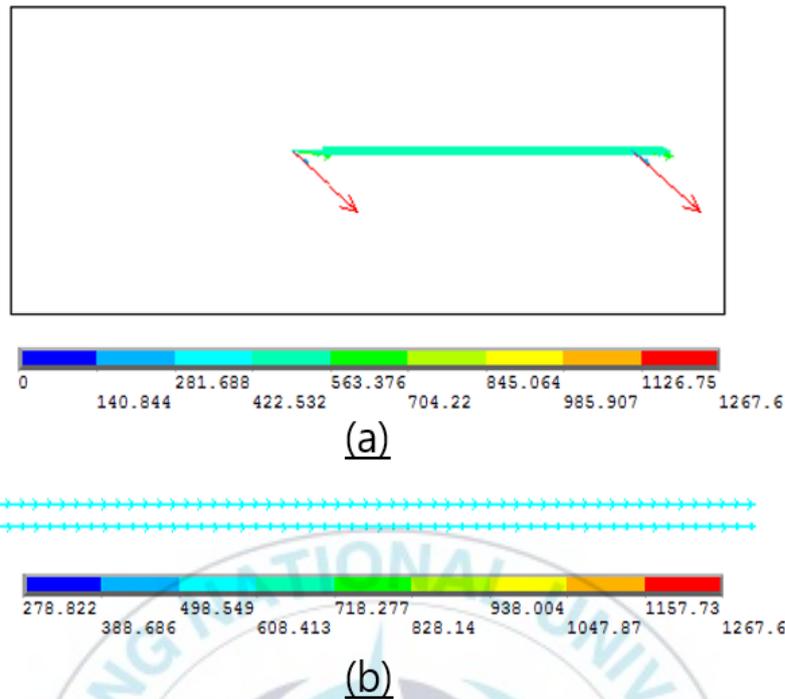
#### 4.1.1 Voltage and current density fields

Figure 4.1 and figure 4.2 show the representative results for the voltage field and the current density field analysis of the PPT. The results for (a) the entire PPT and (b) the heating element are shown in figure 4.1 and 4.2.

Figure 4.1 (a) shows that the other areas except for the heating element are electrically insulated, as shown in figure 2.3. The applied voltage to the heating element is also shown in figure 4.1 (b). The value and direction of the current density formed in the heating element are shown in figure 4.2, and the average of the current density is  $529\text{A}/\text{mm}^2$ .



**Figure 4.1. The voltage fields of (a) the entire PPT and (b) the heating element**

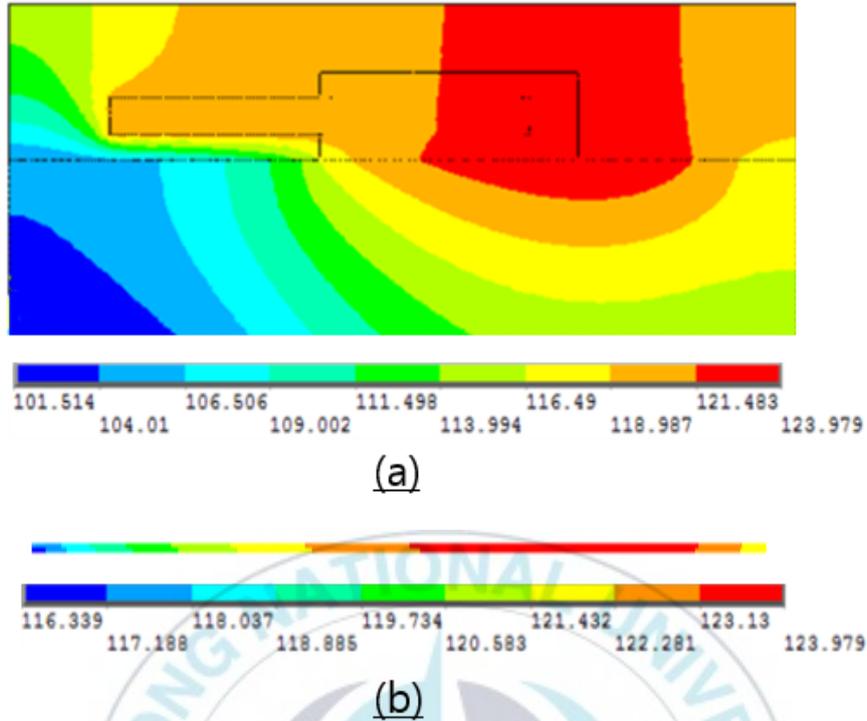


**Figure 4.2. The current density fields of (a) the entire PPT and (b) the heating element**

#### 4.1.2 Temperature fields

Figure 4.3 shows the representative results of the temperature field analysis for (a) the entire PPT and (b) the heating element.

As a result of the analysis, this study qualitatively confirmed that the generated heat rate according to the temperature distribution of the PPT, as shown in figure 4.3 (a), is dissipated to the lower surface of the substrate. The axial temperature gradient of the heating element is 1K/mm as shown in figure 4.3 (b), and this study has been confirmed that the value is significant. Also, it is found that the temperature of the heating element is about 10°C higher than the temperature of the lower surface of the substrate.



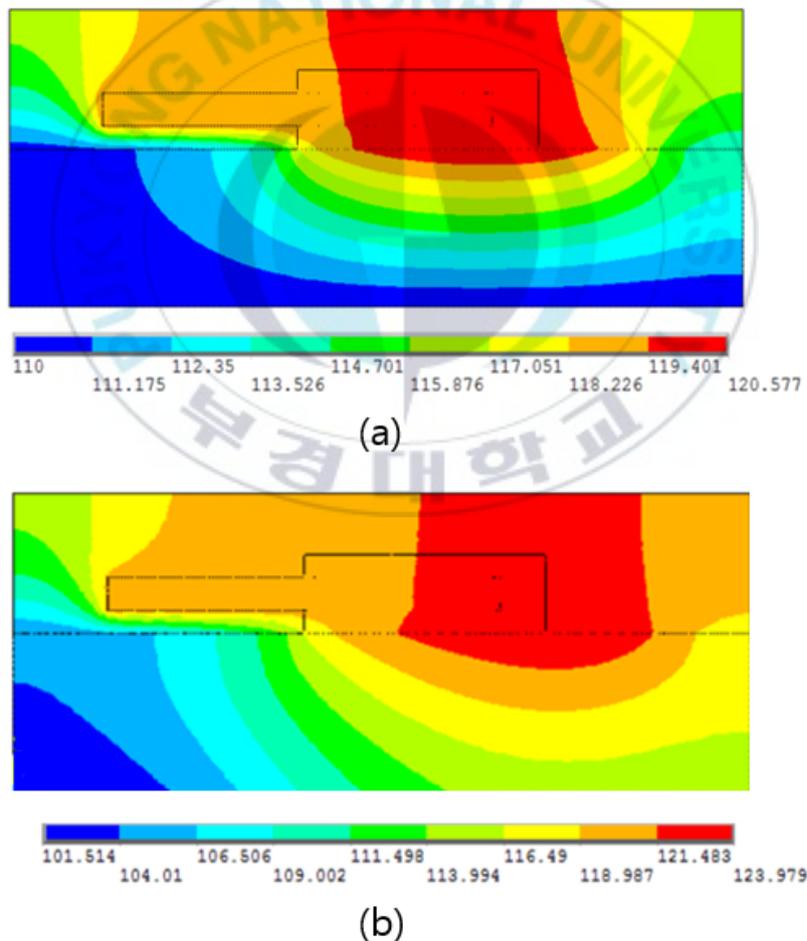
**Figure 4.3. The temperature fields of (a) the entire PPT and (b) the heating element**

#### **4.1.3 Boundary conditions effects**

Figure 4.4 shows the temperature field of the PPT for (a) the isothermal ( $110^{\circ}\text{C}$ ) boundary conditions and (b) the effective heat transfer coefficient ( $3540\text{W}/\text{m}^2 \cdot \text{K}$ ) boundary conditions at the lower surface of the substrate. This study has been carried out to apply the effective heat transfer coefficient boundary conditions similar to the actual situation because the isothermal boundary conditions is very ideal conditions. The effective heat transfer coefficient was applied to the model considering the total power applied to the HP and the average temperature of the lower surface of the substrate,  $110^{\circ}\text{C}$ . After that, the calculated average temperature of the lower surface of the substrate was settled, and the effective heat transfer coefficient was determined

as  $3540\text{W}/\text{m}^2 \cdot \text{K}$  by the trial and error method until the average temperature of the lower surface of the substrate converged in  $110^\circ\text{C}$ .

The results of the boundary conditions show that the maximum temperature of the heating element is  $3.4^\circ\text{C}$  higher than when the effective heat transfer coefficient boundary conditions was applied. This is because the effect of the 2-D thermal diffusion is greater than the isothermal boundary conditions. Therefore, in all of the parametric studies of the PPT, the effective heat transfer coefficient boundary conditions have been applied for heat balance close to the actual situation.

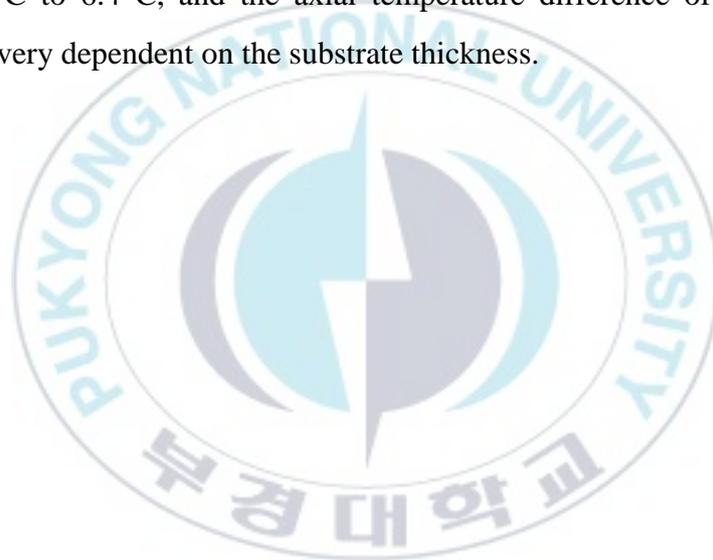


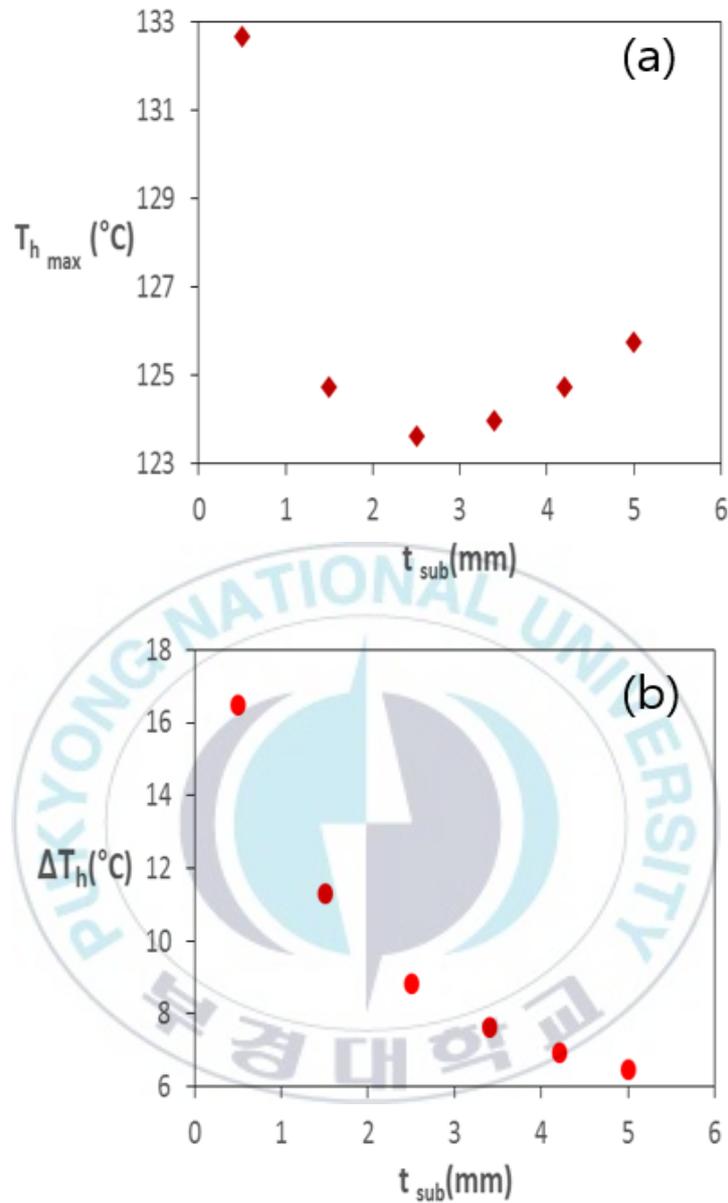
**Figure 4.4. The temperature fields for (a) the isothermal and (b) the effective heat transfer coefficient boundary conditions**

#### 4.1.4 Substrate thickness effects

The results of the maximum temperature ( $T_{h_{max}}$ ) and axial temperature difference ( $\Delta T_h$ ) of the heating element for six cases with the substrate thicknesses ( $T_{sub}$ ) ranging from 0.5mm to 5mm are shown in figure 4.5.

As shown in figure 4.5 (a), the maximum and minimum values for the maximum temperature of the heating element are 132.6°C and 123.6°C, and the discrepancy is 7%. Also, it was found that the maximum temperature of the heating element at the thickness of 2.5mm is the lowest. Figure 4.5 (b) shows that the axial temperature difference of the heating element is reduced by 61% from 16.5°C to 6.4°C, and the axial temperature difference of the heating element is very dependent on the substrate thickness.



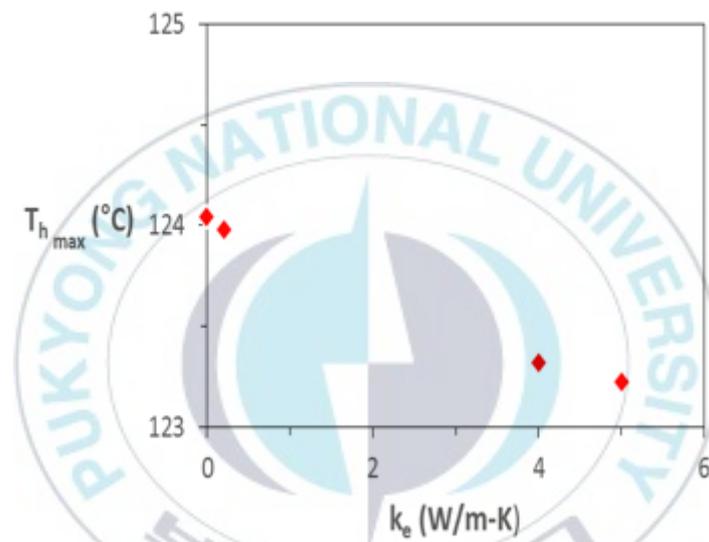


**Figure 4.5. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the substrate thickness**

#### **4.1.5 Encapsulant thermal conductivity effects**

Figure 4.6 shows the maximum temperature of the heating element analyzed when the encapsulant is not present and the encapsulant thermal conductivity ( $k_e$ ) is 0.2W/m-K, 4W/m-K, and 5W/m-K.

Even if the encapsulant thermal conductivity increases from 0.2W/m-K to 5W/m-K, the maximum temperature of the heating element is reduced by 0.6% from 123.9°C to 123.2°C, as shown in figure 4.6. The effects of the encapsulant thermal conductivity on the maximum temperature of the heating element is insignificant. The reason is that most of the generated heat rate is effectively dissipated into the lower surface of the substrate, which is a good thermal conduction layer.



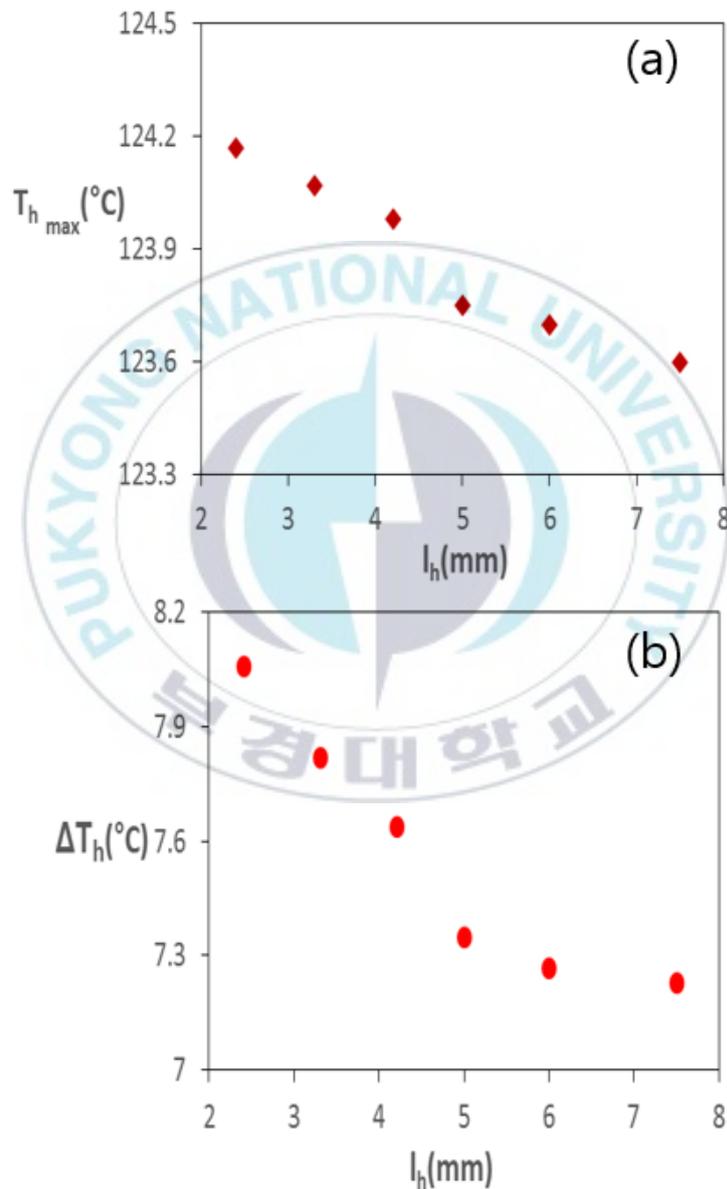
**Figure 4.6. The maximum temperature of the heating element as a function of the encapsulant thermal conductivity**

#### 4.1.6 Heating element area effects

To investigate the effects of the heating element area, the maximum temperature and axial temperature difference of the heating element for the six cases with the contact lengths of the heating element ( $l_h$ ) ranging from 2.4mm to 7.5mm are shown in figure 4.7.

Figure 4.7 (a) shows that the maximum temperature of the heating element decreases from 124.1°C to 123.6°C by 0.5% when the contact length of the heating element increases from 2.4mm to 7.5mm. And figure 4.7 (b) shows that

the axial temperature difference of the heating element is reduced by 10% from 8°C to 7.2°C. In the effects of the heating element area studies, the maximum temperature of the heating element shows a slight reduce, but it shows a meaningful reduce in the axial temperature difference.

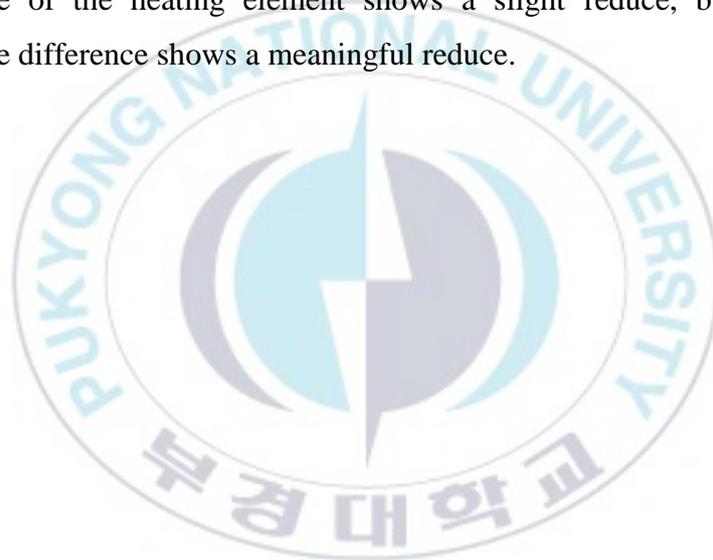


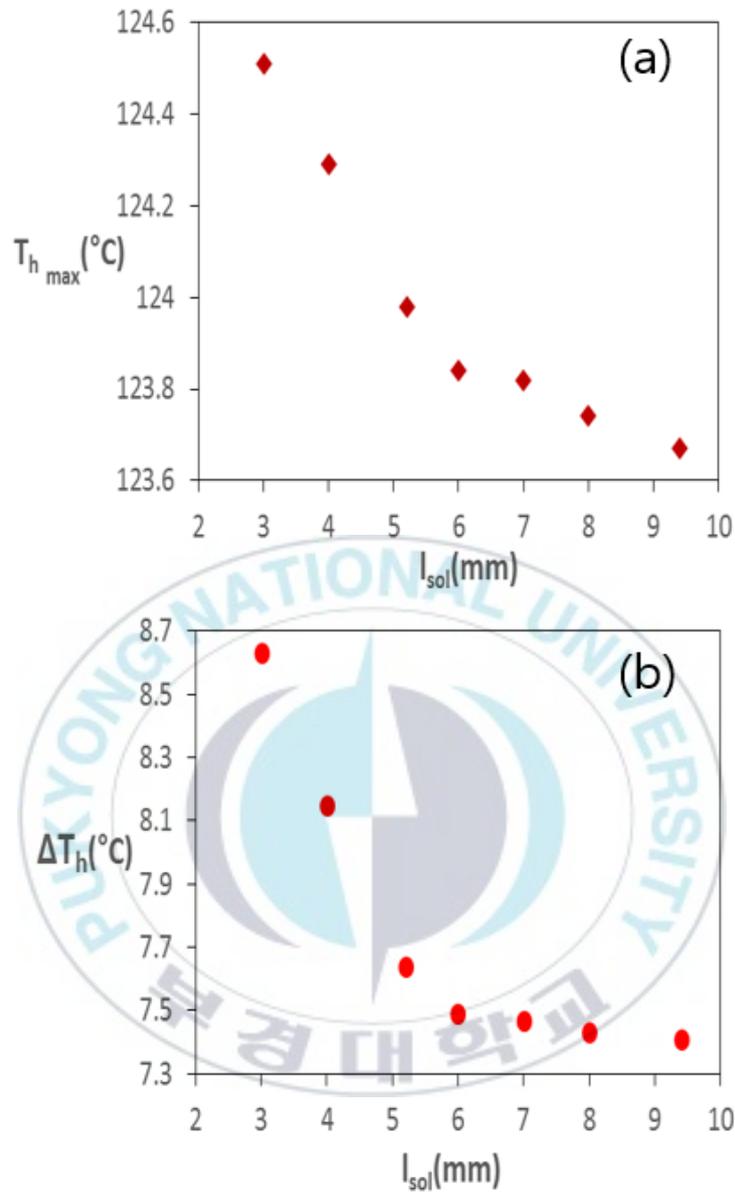
**Figure 4.7. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the heating element area**

#### 4.1.7 Solder contact area effects

The results of the maximum temperature and axial temperature difference of the heating element for seven cases with the solder lengths ( $l_{sol}$ ) ranging from 3mm to 9.4mm are shown in figure 4.8.

Figure 4.8 (a) shows that the maximum temperature of the heating element decreases from 124.5°C to 123.6°C by 0.7% when the contact length of the solder increases from 3mm to 9.4mm. Figure 4.8 (b) is found that the axial temperature difference of the heating element is reduced by 14% from 8.6°C to 7.4°C. In the effects of the solder contact area studies, the maximum temperature of the heating element shows a slight reduce, but the axial temperature difference shows a meaningful reduce.



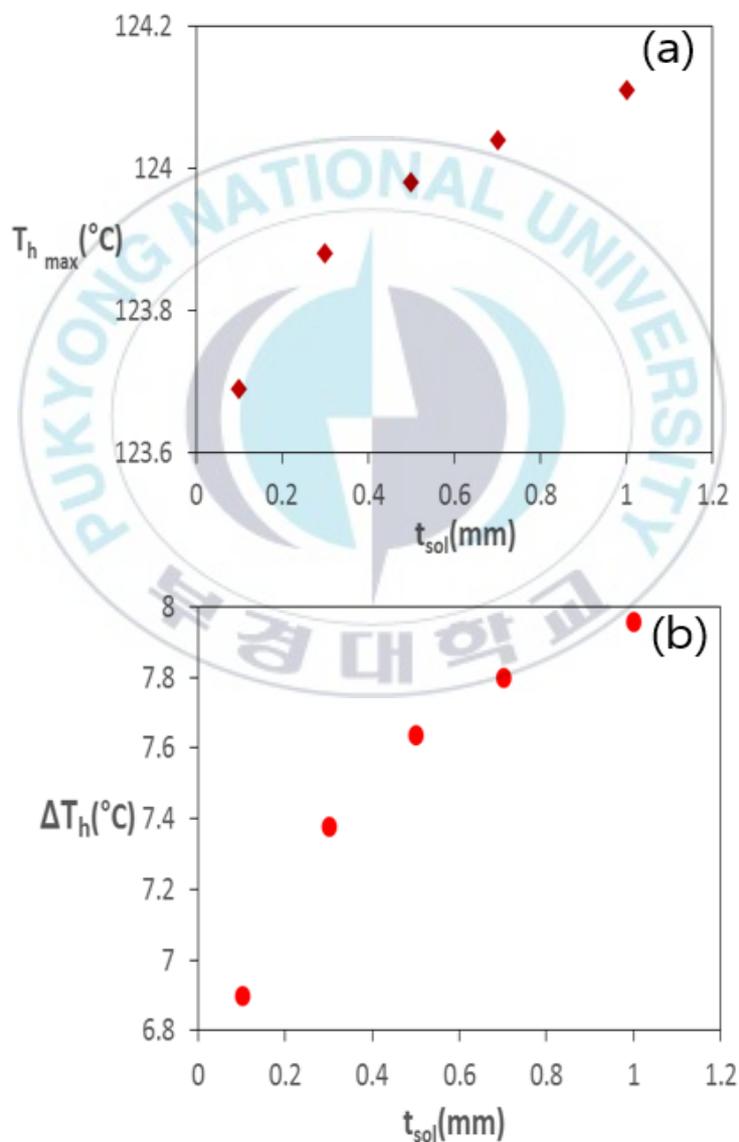


**Figure 4.8. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the solder contact area**

#### 4.1.8 Solder thickness effects

To investigate the effects of the solder thickness, the maximum temperature and axial temperature difference of the heating element for the five cases with the solder thicknesses ( $t_{sol}$ ) from 0.1mm to 1mm are shown in figure 4.9.

Figure 4.9 (a) shows that the maximum temperature of the heating element decreases from 124.1°C to 123.6°C by 0.4% when the solder thickness decreases from 1mm to 0.1mm. The axial temperature difference of the heating element is reduced by 13% from 7.9°C to 6.9°C in figure 4.9 (b). In the effects of the solder thickness studies, the maximum temperature of the heating element shows a slight reduce, but the axial temperature difference shows a meaningful reduce.



**Figure 4.9. (a) The maximum temperature and (b) the axial temperature difference of the heating element as a function of the solder thickness**

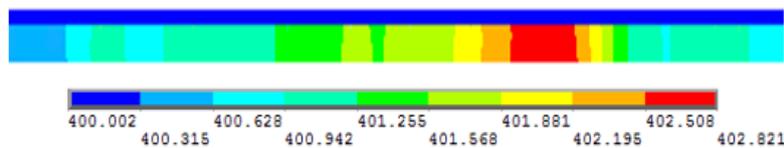
## 4.2 Simulation results of HP

This section discusses the thermal performances of the HP using the FEA thermal model under the dynamic temperature control conditions. The results of the analysis describe the temperature field of the HP on the basic conditions. And also, this section discusses the results of the heating element width, zone and the heating element gap effects on the axial temperature of the upper surface of the HP.

### 4.2.1 Temperature fields

Figure 4.10 shows the analytical result of the temperature field of the HP at 2s for the effective heat transfer coefficient boundary conditions on the upper surface of the air film.

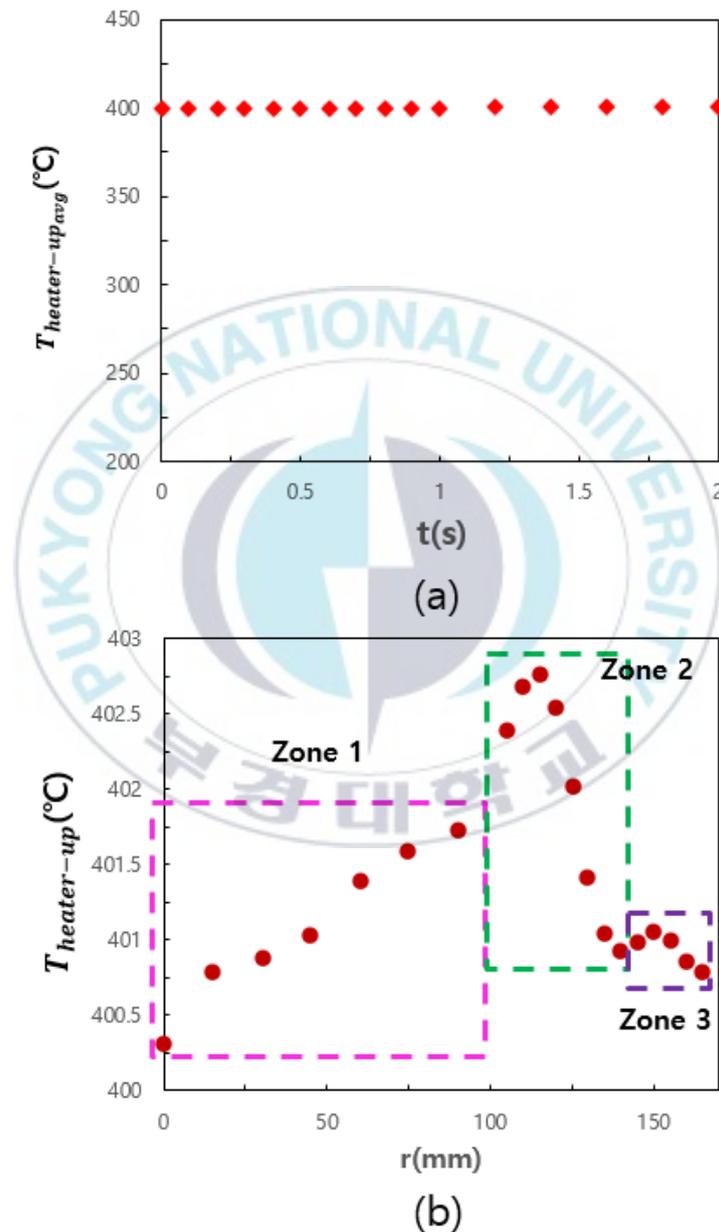
As a result of the analysis, the temperature gradient occurs in the axial direction of the HP, and the temperature is high in the zone 2 where the heating elements are relatively concentrated. Also, this study has been found that the temperature gradient in the wafer rarely occurs because of an ideal thermal boundary conditions.



**Figure 4.10. The temperature field of the HP**

Figure 4.11 (a) shows the average temperature of the upper surface of the HP under the dynamic temperature control conditions. As a result, the average temperature of the upper surface of the HP is steady state. The axial temperature gradient of the upper surface of the HP for the representative analysis results is

shown in figure 4.11 (b). Figure 4.11 (b) shows that there is a maximum temperature difference of  $2.5^{\circ}\text{C}$  in the axial direction of the upper surface of the HP. Therefore, the necessity of studying the temperature uniformity of the HP is confirmed.



**Figure 4.11. (a) The average temperature and (b) the axial temperature of the upper surface of the HP**

#### 4.2.2 Heating element width effects

Figure 4.12 (a) shows the temperature fields of the HP at 2s for the representative three cases of the heating element width effects. [Initial] is the baseline case, and the heating element widths for each zone are 1.4mm, 1.2mm, and 1.8mm. [1mm] is the case when the widths of all heating elements are 1mm, and [2mm] is the case when the widths of all heating elements are 2mm. The applied power to each zone were the same in all cases during the analysis. Figure 4.12 (b) shows the analysis results of the axial temperature of the upper surface of the HP to the effects of the heating element width.

As a result of the analysis, the axial temperature difference of the upper surface of the HP for the [2mm] case is reduced by 5% compared with the [Initial] case. The studies of the heating element width found that the effects of the heating element width on the axial temperature difference of the upper surface of the HP are insignificant. And also, the possibility of simplifying the heating element width is discovered.

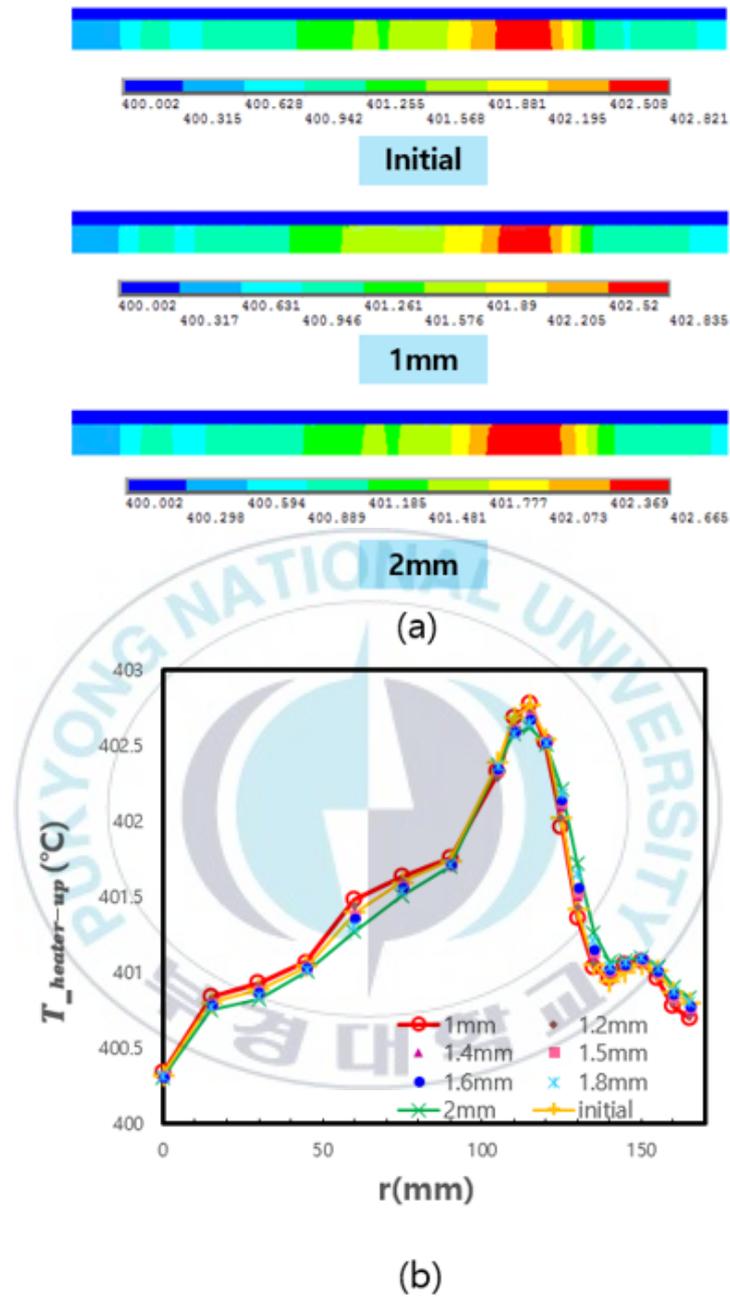
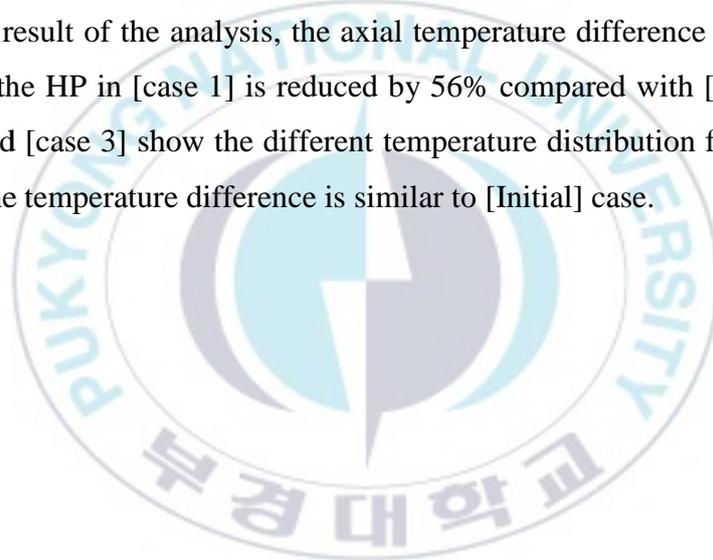


Figure 4.12. (a) The temperature fields of the HPs and (b) the axial temperature of the upper surface of the HP as a function of the heating element width

### 4.2.3 Zone and heating element gap effects

Figure 4.13 (a) shows four cases to investigate the zone and the heating element gap effects. All of the heating element width of [case 1] ~ [case 3] are 2mm. In [case 1], each zone area are the same as [Initial], but gaps of the heating elements are composed of the same lengths for each zone. In [case 2], gaps of all the heating elements are the same. In [case 3], the zone 3 area is the same as [Initial] case, but gaps of the heating elements between zone 1 and zone 2 are the same length, and [Initial] case is the baseline case. Figure 4.13 (b) shows the analysis results of the axial temperature of the upper surface of the HP for the zone and the heating element gap effects in each case.

As a result of the analysis, the axial temperature difference of the upper surface of the HP in [case 1] is reduced by 56% compared with [Initial] case. [case 2] and [case 3] show the different temperature distribution from [Initial] case, but the temperature difference is similar to [Initial] case.



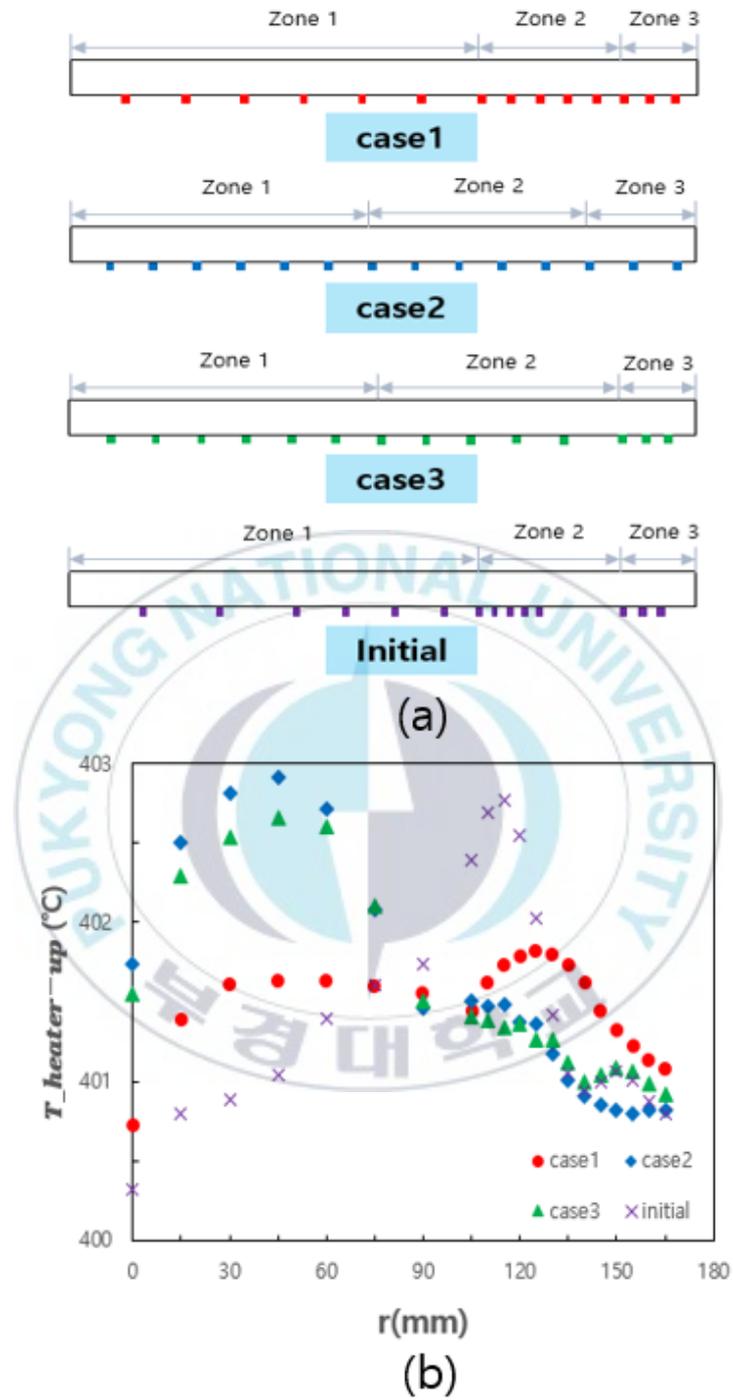


Figure 4.13. (a) The schematics of each case and (b) the axial temperature of the upper surface of the HP as a function of the zone and the heating element gap

## V. Conclusions

In this study, the thermal performances of the PPTs and the HPs have been investigated to analyze and alleviate their thermal failure sources for the wafer thermal processing. First, the FEA electrical-thermal model of the PPT and the FEA thermal model of the HP have been developed by utilizing ANSYS Multiphysics. Second, both models have been experimentally verified. Lastly, the thermal performances and the parametric dependence of the PPT and the HP have been numerically investigated. Experimental verifications of the models show that the maximum discrepancies between measurement and numerical data for the PPT and the HP were less than 3% and 3.7%, respectively.

The primary study results for the PPTs are provided as follows. First, a considerable axial temperature gradient of 1K/mm could be occurred in the heating element, and the average current density was found to be  $529A/mm^2$ . Second, the maximum temperature of the heating element was  $3.4^{\circ}C$  higher with the effective heat transfer coefficient boundary conditions compared with the case of isothermal boundary conditions. Third, it was found that the axial temperature difference of the heating element could be reduced by 61% with the increase of the substrate thickness from 0.5 to 5mm. Fourth, it was shown that the effect of the encapsulant thermal conductivity was negligible; the maximum temperature of the heating element was reduced by only 0.6% despite the increase of its thermal conductivity by 25 times from 0.2W/m-K to 5W/m-K. Finally, it was seen that the effects of the heating element area, the solder contact area, and the solder thickness on the maximum temperature of the heating element was not considerable; the variance of the maximum temperature was smaller than 1%. Nevertheless, the value of the axial temperature difference was reduced by more than 10% with the increase of the heating element area, the solder contact area, and the solder thickness.

The crucial study results for the HPs are shown as follows. First, it was observed that the maximum temperature difference of  $2.5^{\circ}C$  in the axial

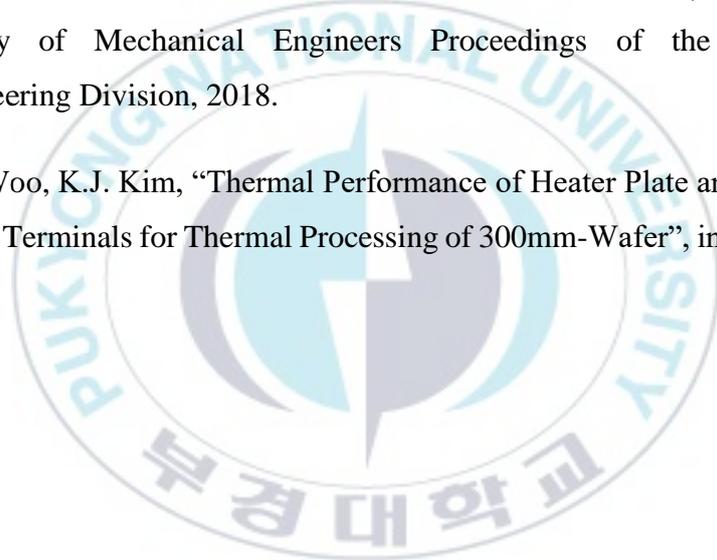
direction of the upper surface of the HP, and the maximum temperature occurring in zone 2. Second, it was found that the axial temperature difference of the upper surface of the HP with a heating element width of 2mm was 5% lower than that of the baseline case. Finally, it was seen that the axial temperature difference of the upper surface of the HP in case 1 was reduced by 56% compared with the baseline case. These results suggest that the optimum thermal design of the structure of the heating element could minimize the adverse effects of thermal factors eventually inducing failures in the PPTs and the HPs and also improve the robustness of the wafer thermal processing.



## List of Publications

1. D.S. Woo, G.Y. Do, B.G. Kim, K.J. Kim, “Numerically-Investigated Thermal Performances of Packaged Power Terminals of Semiconductor Wafer Baking Apparatus”, International Symposium on Advanced Mechanical and Power Engineering, 2016.
2. D.S. Woo, G.Y. Do, B.G. Kim, K.J. Kim, “Electrical-Thermal Analysis of Packaged Power Terminals for Wafer Baking Process”, The Korean Society of Mechanical Engineers Proceedings of the Reliability Engineering Division fall meeting, 2016.
3. D.S. Woo, K.J. Kim, “Multiphysics Thermal Analysis of Heater Power Terminal for Semiconductor Manufacturing”, The Korean Society of Mechanical Engineers Proceedings of the Reliability Engineering Division, 2017.
4. D.S. Woo, G.Y. Do, B.G. Kim, K.J. Kim, “Thermal Performance of Annealing Heater Modules for a Spinner Apparatus”, The Korean Society of Mechanical Engineers Proceedings of the Thermal Engineering Division, 2017.
5. D.S. Woo, G.Y. Do, B.G. Kim, K.J. Kim, “Thermal Analysis of Heater Module for Annealing Process”, 2nd International Joint Conference on Advanced Engineering and Technology & International Symposium on Advanced Mechanical and Power Engineering, 2017.
6. D.S. Woo, K.J. Kim, “Electrical-Thermal-Structural Performance of Packaged Power Terminals for Wafer Baking”, 23rd International Workshop on Thermal Investigations of ICs and Systems, 2017.

7. D.S. Woo, G.Y. Do, B.G. Kim, N.S. Effendi, K.J. Kim, “Thermal Analysis of Heater Modules for Semiconductor Manufacturing”, The Korean Society of Mechanical Engineers Proceedings of the Reliability Engineering Division fall meeting, 2017.
8. D.S. Woo, K.J. Kim, “Electrical-Thermal analysis of Packaged Power Terminals for Thermal Processing of Semiconductor Wafers”, Journal of the Korean Society of Marine Engineering, 2017.
9. D.S. Woo, B.G. Kim, N.S. Effendi, S.S.G.R. Putra, K.J. Kim, “Thermal Analysis of Heater Module for Wafer Thermal Process”, The Korean Society of Mechanical Engineers Proceedings of the Reliability Engineering Division, 2018.
10. D.S. Woo, K.J. Kim, “Thermal Performance of Heater Plate and Packaged Power Terminals for Thermal Processing of 300mm-Wafer”, in preparation.



## References

- [1]. Y. Nishi, R. Doering, "Handbook of Semiconductor Manufacturing Technology", CRC Press, 2007.
- [2]. S.A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, 2001.
- [3]. J. Lee, H.G. Kwon, S. Shin, S. Han, J. Ha, H. Yoo, H.H. Cho, "Thermal design of hat plate for 300-mm wafer heating in post-exposure bake", *Microelectronic Engineering*, vol. 88, no. 11, pp. 3195-3198, 2011.
- [4]. E-A. Khalid, C.D. Schaper, T. Kailath, "Integrated Bake/Chill for Photoresist Processing", *IEEE Transactions on Semiconductor Manufacturing*, vol. 12, no. 2, pp. 264-266, 1999.
- [5]. E-A. Khalid, C.D. Schaper, T. Kailath, "Programmable Thermal Processing Module for Semiconductor Substrates", *IEEE Transactions on Control Systems Technology*, vol. 12, no. 4, pp. 493-509, 2004.
- [6]. H.T. Chua, A. Tay, Y. Wang, X. Wu, "A heater plate assisted bake/chill system for photoresist processing in photolithography", *Applied Thermal Engineering*, vol. 29, no. 5, pp. 985-997, 2009.
- [7]. H.S. Grover, F.P. Dawson, D.M. Camm, Y. Cressault, M. Lieberer, "Application of a Plasma Arc Lamp for Thermal Processing of Semiconductor Wafers", *IEEE Transactions on Industry Applications*, vol. 51, no. 6, pp. 4808-4816.
- [8]. W.K. Ho, A. Tay, C.D. Schaper, "Optimal Predictive Control with Constraints for the Processing of Semiconductor Wafers on Bake Plates", *IEEE Transactions on Semiconductor Manufacturing*, vol. 13, no. 1, pp. 88-96, 2000.
- [9]. P-O. Logerais, O. Riou, F. Delaleux, J-F. Durastanti, "Improvement of temperature homogeneity of a silicon wafer heated in a rapid thermal system (RTP: Rapid Thermal Process) by a filtering window", *Applied Thermal Engineering*, vol. 77, pp. 76-89, 2015.

- [10]. Zhang, Qiaolin, K. Poolla, C.J. Spanos, "Across Wafer Critical Dimension Uniformity Enhancement through Lithography and Etch Process Sequence: Concept, Approach, Modeling, and Experiment" IEEE Transactions on Semiconductor Manufacturing, vol. 20, no. 4, pp. 488-505, 2007.
- [11]. C.D. Schaper, M.M. Moslehi, K.C. Saraswat, T. Kailath, "Modeling, Identification, and Control of Rapid Thermal Processing Systems", Journal of the Electrochemical Society, vol. 141, no. 11, pp. 3200-3209, 1994.
- [12]. Zhang, Qiaolin, P. Friedberg, K. Poolla, C. Spanos, "Enhanced Spatial PEB Uniformity through a Novel Bake Plate Design", AEC/APC XVII, vol. 77, pp. 63-68, 2005.
- [13]. E-A. Khalid, C.D. Schaper, T. Kailath, "Control of spatial and transient temperature trajectories for photoresist processing", Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, vol. 17, no. 5, pp. 2109-2114, 1999.
- [14]. A. Tay, W.K. Ho, N. Hu, "An In Situ Approach to Real-Time Spatial Control of Steady-State Wafer Temperature During Thermal Processing in Microlithography", IEEE Transactions on Semiconductor Manufacturing, vol. 20, no. 1, pp. 5-12, 2007.
- [15]. T.K. Lim, S.H. Rhi, "Experimental study on nanofluidic heat pipe hot chuck plate in semiconductor wafer baking process", Journal of Mechanical Science and Technology, vol. 24, no. 7, pp. 1501-1509, 2010.
- [16]. K.V. Ling, W.K. Ho, B.F. Wu, A. Lo, H. Yan, "Multiplexed MPC for Multizone Thermal Processing in Semiconductor Manufacturing", IEEE Transactions on Control Systems Technology, vol. 18, no. 6, pp. 1371-1380, 2010.

- [17]. ANSYS Multiphysics User's Guide, ANSYS Inc., 2016.
- [18]. M.N. Ozisik, "Heat Conduction", John Wiley and Sons Inc., 1993.
- [19]. A.R. Hambley, "Electrical Engineering: Principles & Applications"  
Prentice Hall Inc., 2010.

