Dissertation for the Degree of Doctor of Philosophy

Development of High-Linearity CMOS RF Front-End Technology for Automotive Collision Avoidance Radar

by

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Pukyong National University

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높은 선형성을 가진 차량충돌 방지 레이더용 CMOS 고주파 전단부 개발

Advisor: Prof. Jee-Youl Ryu

by

Murod Kurbanov

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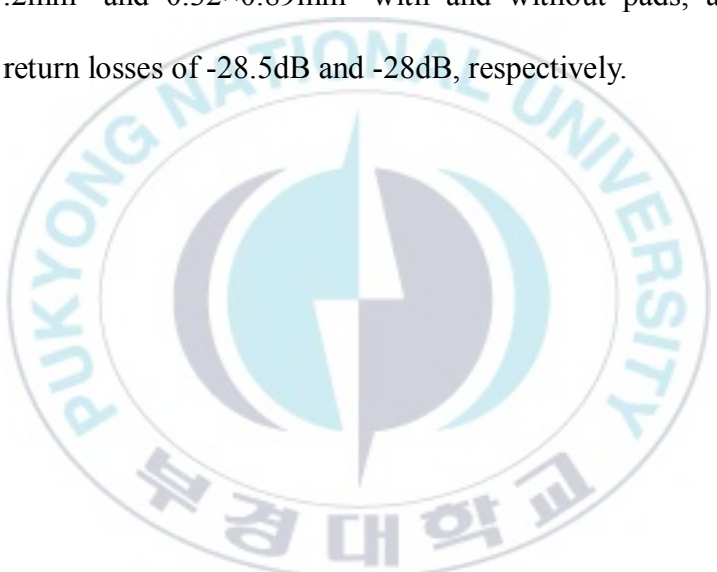
ABSTRACT

In recent issues, an RFIC is being more popular due to stability, compactness, and small dimension. Especially, an RF circuit in the mm-wave band is convenient to design it from the spectrum regulations and technology availability. Transceiver design in CMOS technologies is always a matter of challenges to get higher performance. The demand of RF frontends increases which should be firmly incorporated with analog, digital, and mixed signal hardware. However, the reliability of the incorporated RF frontend receiver keeps on involving significant concern and impressive research.

In this thesis, we propose a new approach of design and performance analysis of an RF frontend receiver. It consists of a differential low noise amplifier (LNA) and, a down-conversion mixer for automotive collision avoidance radar application. The LNA and mixer is designed and implemented using 65nm RF CMOS technology with the supply voltage of 1.5V at 24GHz. The LNA is designed with cascode inductive source degeneration technique. The bias offset method is adopted in mixer design to boost its conversion gain and to reduce power consumption. This RF frontend receiver is improved by features with a trade-off between linearity and gain. The work is performed on Cadence Virtuoso design and

simulation platform.

The proposed frontend showed very high third-order input intercept point (IIP3) of 4.3dBm to verify excellent linearity. The circuit also showed high conversion gain of 28.1dB, low noise figure of 3.66dB, and a very low power consumption of 6.03mW. This frontend showed a small die area of $0.80\times1.2mm^2$ and $0.32\times0.89mm^2$ with and without pads, and input and output return losses of -28.5dB and -28dB, respectively.



Chapter 1

1. Introduction

1.1. Motivation

Road traffic collisions have become a significant global concern over the past few years. To increase road safety and comfort by informing the driver for obstacles or slowdowns on the road, automotive collision avoidance radar applications are being implanted on a lot of transport systems and deluxe passenger cars for many years. During the last decade, so many researches have been conducted in 24GHz and 77GHz band radars [1], [2]. For the sake of detection of other near vehicles in the medium-short range and wide beam, 24GHz is the main stream in the design of an automotive collision avoidance radar. In fact, this choice of frequency involves trade-offs between several factors such as transmitted power and received power [3]. The advanced cruise control (ACC) introduces automotive radar, it consists of two types of radar such as short range radar (SRR) and long range radar (LRR) [4].

1.2. Short-Range Radar and Long-Range Radar

Figure 1.1 shows that the opening angles for each one of the two types of radar are different. It goes from 30° to 180° in the case of the SRR

whereas a value of lower than 10° is generally required for the LRR. The SRR aims to detect objects in the immediate vicinity of the vehicle with a detection distance of up to 30 meters in maximum. This radar is intended to warn the driver for the risk of collisions. It can be coupled to passive safety systems that can be triggered such as pre-crash detection, parking aid side object detection and blind spot detection. It also provides information on obstacles in blind spots detection during lane changes, and it can help with parking. Finally, systems provide recognition of traffic signs and the detection of pedestrians on road. The LRR provides the capability to complement the SRR capability by allowing detection of upstream vehicles to maintain a minimum safe distance on the road. The LRR works in pulse mode with a covered distance of approximately 200 meters.

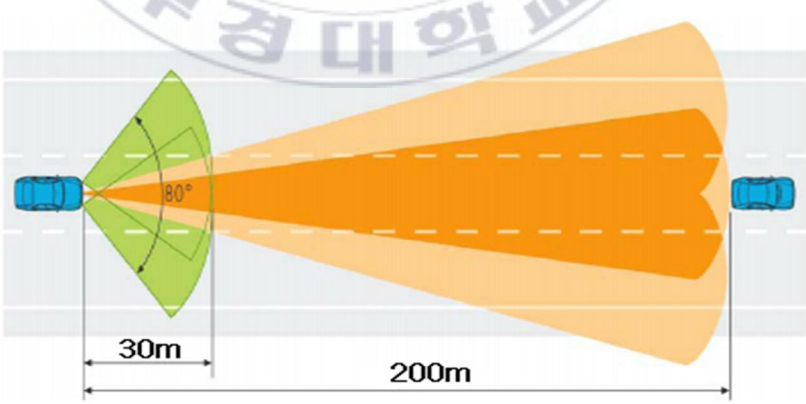


Figure 1.1. Combination of SRR and LRR

Figure 1.2 shows all applications for automotive collision avoidance

radar, the radar aims to improve the safety of drivers, and to anticipate driving in case of danger. The radar also controls the braking system and steering wheel to save the people's life, and reduce the severity if collisions. Future generations of vehicles should be able to communicate with each other for their relative positions, and to alert each other for traffic status or weather. In near future, all applications should be developed at 24GHz and 77GHz. All of these predictive security applications are part of the Intelligent Transportation System (ITS) at 24GHz [5].

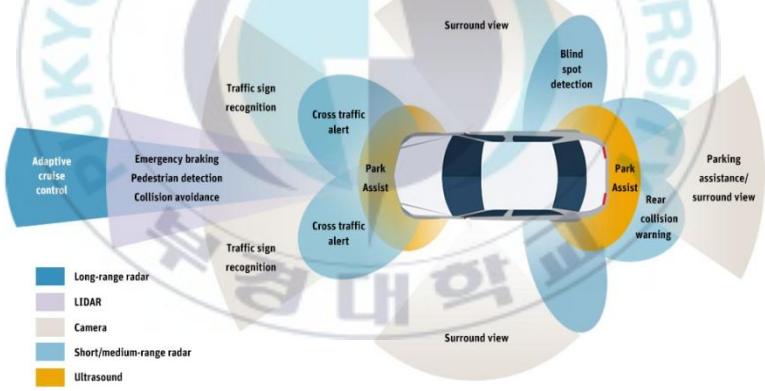


Figure 1.2 Possible application for automotive radar

1.3. Proposed Frontend Receiver Architecture

Several silicon technologies are eligible for millimeter-wave

applications. CMOS technology achieves a high level of integration. BiCMOS technology is more complex than CMOS technology. The schematic frontend receiver is shown in Figure 1.3. The transmitted signal from the antenna has a very low power level since the wireless communication provides a lot of losses in long distance. In a receiver, an LNA is used after antenna to amplifier voltage level of the received signal [6]. The mixer is used to convert the amplified signal into the desired lower frequency to enable channel filtering. The mixer also effectively multiplies the signal to another signal provided by a local oscillator (LO).

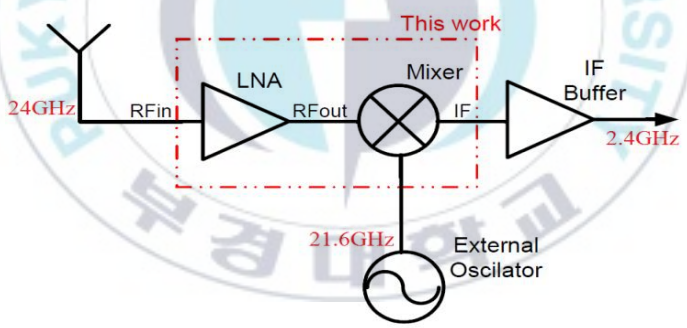


Figure 1.3 Frontend receiver

Figure 1.4 shows basic mixing principle for the mixer. In the mixer, a modulated RF signal is inserted, while a second signal from the LO performs the frequency transposition. At the output, an intermediate frequency (IF) signal contains the sum and difference frequencies of $f_{RF}+f_{LO}$

and f_{RF}-f_{LO}. The principle of a mixing requires the use of nonlinearities of components to realize the conversion into lower frequency. The nonlinear mixer is able to apply at any frequency where the device presents a known nonlinearity. At low frequencies excellent switches can be realized, so the switching mode mixer is preferred because it generates lesser spurs. These nonlinearities are controlled by the amplitude of the signal.

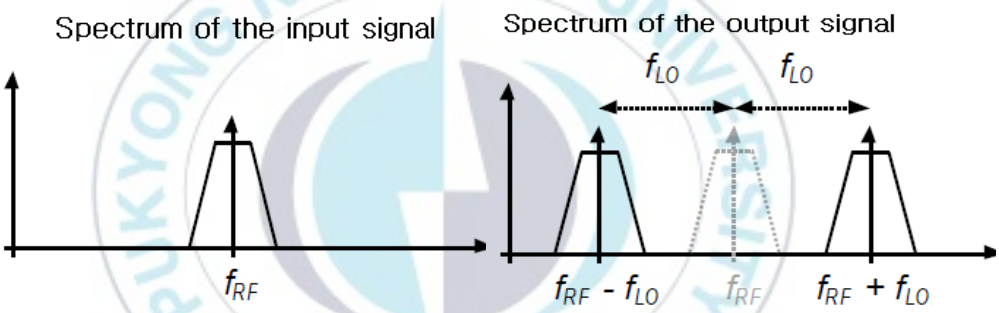


Figure 1.4 Basic principle of the frequency conversion

1.4. Objective

The main objective of this work is to design RF front-end receiver with a low noise amplifier(LNA) and mixer using 65nm RF CMOS technology for 24 GHz automotive radar [7]. This front-end receiver provides short distances applications. The conventional building style of RF front-end receiver is generally merged and coupled jointly with matching

network, filters, or balun. This study reports low-power and high-linearity fully-differential LNA connected to downconversion mixer. The objectives of this work are as follows:

- To design a new RF front-end receiver architecture to perform the collision avoidance. Due to a low-power and low-cost issue, the RF receiver is the best among the different architectures. The leakage, mismatch, and flicker(1/*f*) noise from local oscillation(LO) are several issues of the receiver. To solve these issues, the double balanced mixer architecture of single intermediate frequency(IF) is proposed. Initially, the incoming signal is converted into an IF in this type of receiver, and then it is converted into a baseband frequency again. This process softens the receiver back-end requirements and allows low-frequency analog-to-digital conversion.
- To prove the validity of each block in the receiver frontend, a set of new mathematical formulas is given.
- New LNA has been designed, implemented, laid out, and finally fabricated. The designed LNA has unique structure and its features have been proved by mathematical equations and the measurement results.
- The second block in front-end receiver is downconversion mixer.

LNA and mixer are combined to reduce the power consumption and to increase the linearity of the overall receiver. The mixer circuit is employed in an IF receiver(*IF downconversion mixer*) to reach the predefined characteristics such as low noise and low power consumption.

1.5. Overview

The study is structured as follows. The first block in the receiver front-end, known as the low noise amplifier(LNA) is introduced in Chapter 2. The background of LNA is presented, and then the fundamental features of LNA are defined. These fundamental characteristics assist the readers to get LNA parameters, and present trade-offs between the output effects of LNA which provide at the end of this chapter. After this, the new concept of LNA is proposed and proved with mathematical equations as well. The measurement outcomes verify the validity of the newly designed circuit for RF applications. The design of layout and die microphotograph of the proposed LNA is additionally presented. The evaluation of the proposed concept as compared with the conventional research results is given as well [8].

The definition and clarification of downconversion mixer is addressed in Chapter 3. Various types of active mixer configurations are

discussed with their advantages and disadvantages. The new mixer structure is established to achieve the predefined parameters such as noise figure(NF), conversion gain, and power consumption at the end of Chapter 3.

The complete front-end receiver is discussed in Chapter 4. The different blocks of the receiver chain on a single chip are assembled together in this chapter. Each block of LNA and mixer is analyzed in detail and clarified. At the end of this chapter, the results of the proposed front-end with a high level of integrity are shown. Additionally, we show the layout and die microphotograph of the receiver front-end [9], [10].

Chapter 2

2. Overview and Design of Low Noise Amplifier

2.1. Background

The most demanding component is the low noise amplifier(LNA), which is normally the first component in RF receiver. At the same time, it must meet several specifications that make its architecture difficult. The signal from the receiver antenna at the input of the LNA is very low and typically ranges from under -130dBm(for GPS signals) to -70dBm. Therefore, the LNA amplifies these signals without creating any noticeable disruption to the handling of the following stage such as mixer and filter. It sets the LNA's requirement for a certain benefit. The sensitivity of the receiver chain is further determined by the sensitivity to the LNA [11]. This needs that the overall receiver must be integrated with minimal noise from the LNA. Based on IEEE standards, there are specific input/output termination impedances, i.e. 50Ω or 75Ω on the LNA. LNA noise is a function of source impedance as well. It's noteworthy that the optimum source impedance for minimum noise figure from the one is required for the input impedance of the preceding stage with 50Ω [12].

Therefore there are trade-offs between gain, noise figure, and input/output matching impedance. The LNA sets the receiver's minimum noise number based on Friis' equation. The Friis' equation is used to measure a successive system's total noise figure, and each stage with its noise figure and gain. The Equation (2.1) expresses the total noise figure [13].

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_n} \quad (2.1)$$

where the F_i and G_i are a noise figure and gain of the i_{th} stage, respectively. Because of this equation, a receiver's total noise is mainly dominated by the first stage of the system when the LNA has high voltage gain(G_1). As expressed in Equation (2.2), the noise of subsequent stages degrades by LNA gain.

$$F_{receiver} = F_{LNA} + \frac{F_{rest} - 1}{G_{LNA}}, \quad (2.2)$$

where F_{rest} is a noise figure of next stage. Therefore, the LNA provides adequate gain to transcend the noise of the next stages, although it can compromise the receiver's sensitivity. The significant problem as well as the noise figure and gain is sufficiently wide bandwidth [14], [15]. To cover the entire reception band with a certain margin of size, but narrow enough to

eliminate unwanted interferers, only a good input impedance matching with source input is needed to fulfill LNA's filtering function. In addition, overall front-end or receiver linearity efficiency usually depends on the linearity of this stage(LNA). Linearity such as bandwidth should be adequate to accommodate broad blockers and not to create undesirable intermodulation tones within the band being considered.

Therefore, there are many conditions to be fulfilled to build a proper LNA. While meeting all specifications together is difficult due to simultaneous parameter optimization, designers need to find solutions according to their own desires. A great number of different topologies of LNA are already presented in open literatures.

2.2. S-Parameter

Scattering parameters usually called by S-parameter are widely used in the design and study of microwave and RF circuits. In S-parameter a set of parameters is used which is connected to the moving vibrations that are scattered or mirrored whenever an n-port network is placed in a transmission line.

To characterize an n-port linear network, S-parameter analysis is basically used as a modelling method. H-parameter, Y-parameter, and Z-

parameter are other methods to characterize the n-port network. Since they are behavioral modelling methods, we can put all of them into the same category for a network. The device or n-port network is assumed as a black box, and only the interaction between the ports and outer environment is modelled. For example, H-, Y-, or Z-parameter are commonly used in low frequencies, because voltage and current are the variables for finding the transfer function. However, if we want to use H-, Y-, or Z-parameter, some problems arise for relatively high frequencies.

It is difficult particularly for RF bands to apply short and/or open circuit conditions at each port in H, Y or Z measurement. In stable short or open circuit settings, active devices such as transistors and tunnel diode are not most often connectable.

On the other hand, S-parameters are typically measured with the system embedded between a load and a source of 50Ω, so oscillations are very unlikely to occur. The main advantage of S-parameter is that the moving waves do not differ in magnitude at every points along a lossless transmission line, unlike terminal voltages and currents. This ensures that S-parameter can be calculated at a distance from measuring transducers on a system.

The behavior of the two-port network in Figure 2.1 can be described by

the linear equations using S-parameter as defined in Equations (2.3) and (2.4).

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.3}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.4}$$

where a_1, a_2, b_1 and b_2 are traveling waves.

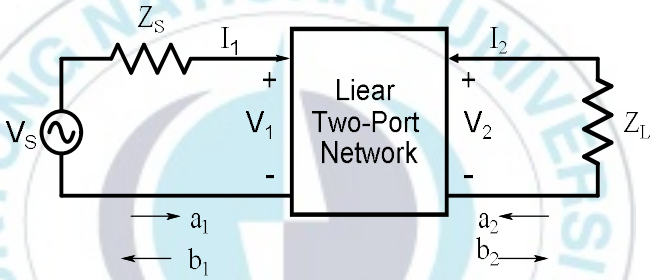


Figure 2.1. Two-port network with incident waves (a_1, a_2) and reflected waves (b_1, b_2)

The S-parameter is defined as Equations (2.5)~(2.8).

$$S_{11} = \frac{b_1}{a_1}|_{a_2=0} \tag{2.5}$$

$$S_{22} = \frac{b_2}{2}|_{a_1=0} \tag{2.6}$$

$$S_{21} = \frac{b_2}{a_1}|_{a_2=0} \tag{2.7}$$

$$S_{12} = \frac{b_1}{a_2}|_{a_1=0} \tag{2.8}$$

For simplicity in measurement and calculation, we assume that the input and the output are both real and positive, and have same reference impedance of Z_0.

The independent variables a_1, a_2, b_1 and b_2 can be related to port voltages (V_1, V_2) and currents (I_1, I_2) as expressed in Equations (2.9)~(2.12).

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{i1}}{\sqrt{Z_0}} \tag{2.9}$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{i2}}{\sqrt{Z_0}} \tag{2.10}$$

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{r1}}{\sqrt{Z_0}} \tag{2.11}$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{r2}}{\sqrt{Z_0}} \tag{2.12}$$

where $V_{i1} = \frac{V_1 + I_1 Z_0}{2}$ and $V_{i2} = \frac{V_2 + I_1 Z_0}{2}$ are incident voltage waves on port 1 and port 2, respectively. $V_{r1} = \frac{V_1 - I_1 Z_0}{2}$ and $V_{r2} = \frac{V_2 - I_2 Z_0}{2}$ are both mirrored voltage waves from port 1 and port 2.

$|a_1|^2$ is the occurrence power at the input of the system and the available source impedance power Z_0. $|b_1|^2$ is the power reflected from the

network port in input port, or the available power from a Z_0 source minus the power supplied to the network. $|a_2|^2$ is the incident power on the network in output, and also the reflected power from load. $|b_2|^2$ is the power reflected from the network in output port, or the incident power on the load, which is also the power supplied to the Z_0 load.

The expressed S-parameter related to the mentioned definition of a_1, a_2, b_1 and b_2 are as follows:

$$|S_{11}|^2 = \frac{Refelected\ power\ from\ input\ network}{Incident\ power\ on\ the\ input\ network} \tag{2.13}$$

$$|S_{22}|^2 = \frac{Refelected\ power\ from\ output\ network}{Incident\ power\ on\ the\ output\ network} \tag{2.14}$$

$$|S_{21}|^2 = \frac{Power\ deliverd\ to\ Z_0\ load}{available\ power\ from\ Z_0\ source} = Transducer\ power\ gain\ with\ Z_0 load\ and\ source \tag{2.15}$$

$$|S_{22}|^2 = Reverse\ trabsducer\ power\ gain\ with\ z_0 \text{ load and source} \tag{2.16}$$

2.3. Gain

The input/output impedance matching network and RF transistor are the parameters that determine and control the gain performance for an RF amplifier such as LNA. The amplifier is modeled by its S-parameter and terminated by arbitrary source and load impedance, Z_S and Z_L. S_{11} and S_{22}

are the input and output reflection coefficients with Z_0 source and load terminations, respectively.

The voltage gain is defined as Equation (2.17).

$$A_v = \frac{V_{out}}{V_{in}} \tag{2.17}$$

The output voltage of a load impedance is $V_{out} = I_{out}Z_L$, and I_{out} is the output current at input stage, so the voltage gain can be presented as Equation (2.18).

$$A_v = \frac{V_{out}}{V_{in}} = \frac{I_{out}Z_L}{V_{in}} = g_{m,eff}Z_L \tag{2.18}$$

2.4. Stability Factor

Stability is also a very important parameter of RF amplifier. The other parameters such as gain, noise figure are meaningful when the amplifier is stable. By assuming the input impedance at the input port of the amplifier $Z_i = R_i + jX_i$, then the Γ_{in} is expressed in Equation (2.19).

$$\Gamma_{in} = \left|\frac{Z_i - \mathrm{Z_0}}{Z_i + \mathrm{Z_0}}\right| = \sqrt{\frac{(R_i - Z_o)^2 + X_i^2}{(R_i + Z_o)^2 + X_i^2}} \tag{2.19}$$

If the real part of the input resistance R_i is negative, i.e. $R_i < 0$, then $|\Gamma_{in}| > 1$. Oscillation can occur if the loss comes from the input termination

network compensated by negative resistance. The amplifier is potentially unstable. We have same scenario for the stability issue of output port. Therefore, the amplifier is unconditionally stable if for all the passive terminations at the input and output ports, Equations (2.20a) and (2.20b) would be satisfied. Otherwise, it is potentially unstable or conditionally stable.

$$|\Gamma_{in}| < 1 \tag{2.20a}$$

$$|\Gamma_{out}| < 1 \tag{2.20b}$$

In term of S-parameter, it can be expressed that the amplifier are unconditionally stable if it has the following conditions.

$$|S_{11}| < 1 \tag{2.21a}$$

$$|S_{22}| < 1 \tag{2.21b}$$

$$K > 1 \tag{2.22}$$

where *K* is the stability factor given by Equation (2.23).

$$K = \frac{1 - |S11|^2 + |S22|^2 + |S11 * S22 - S12 * S21|^2}{2|S12 * S21|} > 1 \tag{2.23}$$

Adding a shunt conductance or a series resistance to the unstable port is the simple method to stabilize an active device. Practically, since the input

and output ports of the amplifier are coupled to the other, it is usually enough to stabilize one of the ports. One should not add a series resistance or a shunt conductance to the input port of the amplifier, since it will cause additional noise to be amplified. Therefore, the best way is to stabilize the output port.

2.5. Noise

This is a factor that makes it possible to assess the quality of a device according to the noise. In fact, it allows to quantify the noise level in a signal, and this factor becomes more and more important when dealing with low input powers. There are various noise sources with varying noise generation. Within the integrated circuits shot noise, flicker noise, and thermal noise are the primary sources of noise. The noise from the shot is generated primarily, and it is unique to nonlinear devices such as field - effect transistors through jumping electrical charges over a semiconductor. In MOS systems, the dc gate leakage current is the only source of shot noise, and is therefore not considered a major problem [16]. The shot noise in base and collector is the key sources in the bipolar junction transistor (BJT), and they can dramatically reduce the improved receiver performance.

There is flicker noise known as pink noise, and it comes up because

charges are caught in channel area defects and impurities in MOS devices [17], [18]. As can be seen from the Equation (2.24), flicker noise is directly proportional to the wavelength of operations (*f*). In the other words, larger MOS devices with large *W* lead to less flicker noise. Equation (2.24) determines the spectral density of this noise.

$$\overline{i_{fn}^2} = \frac{K.g_m^2}{fWLC_{ox}{}^2} \tag{2.24}$$

where *K* is a device geometric constant, the width and length of the MOS device is *W* and *L*, respectively. C_{ox} is the gate-oxide capacitance per unit area, and g_m is the trans-conductance of the MOS device [19].

Therefore, at very low frequencies the dominant noise source is flicker noise. Flicker noise plays significant role in LNAs because the frequency range of the received signal is several gigahertzes, and hence it can be ignored [20]. It is noteworthy that in mixers or voltage-controlled oscillators (*VCOs*) flicker should be considered and can be a serious issue.

2.5.1. Noise Sources

Figure 2.2 illustrates the standard small signal model of a cascode configuration with noise sources. Four sources of noise have been measured: the thermal source resistance noise ($i_{n,Rs}$), thermal channel–current noise ($i_{n,d}$), the current noise caused by the gate ($i_{n,g}$), and the thermal noise of the

output resistance ($i_{n,out}$). The spectral density of power (*SDPs*) of $\overline{i^2_{n,Rs}}$ and $\overline{i^2_{n,Rout}}$ are as follows:

$$\overline{i^2_{n,Rs}} = 4KT\frac{1}{R_s}\Delta f \tag{2.25}$$

$$\overline{i^2_{n,Rout}} = 4KT\frac{1}{R_{out}}\Delta f \tag{2.26}$$

where T is absolute Kelvin temperature, the noise frequency in Hz is Δf and the Boltzmann constant is K.

The SDPs for channel-current thermal and gate-induced noises given by Equations (2.27) and (2.28) [21].

$$\overline{i^2_{n,d}} = 4KT\gamma g_{d0}\Delta f \tag{2.27}$$

$$\overline{i^2_{n,g}} = 4KT\delta g_g\Delta f \tag{2.28}$$

where g_g is the equivalent conductivity of shunt gate given by [22].

$$g_g = \frac{(\omega C_{gs})^2}{5g_{d0}} \tag{2.29}$$

where g_{d0} is drain conductance *of zero drain source voltage,* and γ is a parameter y-dependent on technology *with* a ratio of approximately 2/3 for long-channel devices in the saturation region (in short-channel devices γ is

greater *with* between 2 and 3) [23]. δ is the noise coefficient of the gate, and is also a parameter depending on technology. The importance is 4/3 for long channel devices, and is decreased in short channel devices by a factor of 2.

2.5.2. Noise Figure

We define the noise figure of a device as being the ratio of the noise power available at the output of the device compared to the part of this power due to the internal impedance of the source placed at the input and assumed to be carried at a temperature of *290° K*. In other words, the noise figure is the degradation due to the component of the signal-to-noise ratio (*SNR*) of the source, assumed to be raised to *290° K*. This is therefore the ratio between the *SNR* at the input of the device and the *SNR* at the output of the device.

$$NF = \frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{N_{out}}} = \frac{SNR_{in}}{SNR_{out}} = \frac{total\ \ output\ \ noise\ \ power}{output\ \ noise\ \ power\ \ due\ \ to\ \ source} \tag{2.30}$$

where SNR_{in} and SNR_{out} are respectively the signal-to-noise ratio measured at the input and the output of the device. S_{in} and N_{in} are the input noise and signal powers while S_{out} and N_{out} represent the output noise and signal

powers, respectively.

The NF can be defined in two ways for each block separately or the entire receiver. LNA noise which is known as NF_{LNA} determines inherent noise, and it is added to the desired or wanted signal during the process of amplification.

According to the classical two-port network, NF of a noisy two-port network can be written as Equation (2.31).

$$NF = NF_{min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - b_{opt})^2] \quad (2.31)$$

where NF_{min} is the attainable minimum NF, B_{opt} and G_{opt} are NF_{min}'s, ideal source susceptibility and conductance, respectively. R_n is equal to noise resistance that quantifies NF's ability to deviate from ideal parameters.

The NF is a source admittance function seen from the input terminal of two-port network. An optimum entry, namely Y_{opt}, should be inserted into the network to attain the NF_{min}. The NF_{min} and Y_{opt} expressions for a MOS device can be derived by considering a two-port network configuration for the MOS system. In this model the input port is the gate-source terminal, and the output port is the drain-source terminal.

A small signal model of a MOS device which consists of all noise sources connected to the noise source $\overline{i_s^2}$ and the source admittance

$Y_s=G_S+jB_s$ is shown in Figure 2.2.

We assume that in MOS devices $\overline{i_{n,g}^2}$ and $\overline{i_{n,d}^2}$ are dominant noise sources and the following expressions for the noise parameters and NF_{min} can be obtained [24].

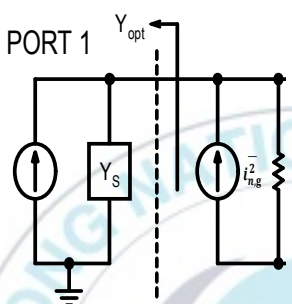


Figure 2.2. Two-port MOS network configuration for measuring the noise.

$$R_n = \frac{\gamma g_{d0}}{g_m^2} \tag{2.32}$$

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{2.33}$$

$$G_{opt} = -\omega C_{gs}(1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \tag{2.34}$$

$$NF_{min} \approx 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_t}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{2.35}$$

where $\alpha = g_m/g_{d0}$ and for long channel devices it is equal to one, and

decreases as devices shrink to smaller dimensions.

It is obvious from Equation (2.35) that with the increasing transition frequency (f_t) the minimum noise figure decreases. It should be noted that as CMOS is scaling down, the transient frequency increases. Therefore, employing CMOS technology will be an advantage to provide low noise figure [25].

2.5.3. First-stage Output Noise

Section 2.7 will describe the input impedance of the inductive source degeneration technique in the cascode. Figure 2.3 shows small signal model of a cascade topology with inductively degenerated noise source.

The input impedance should be equal to the impedance of the source, *Rs*, and could be expressed as Equation (2.36).

$$Z_{in} = \mathrm{g}_m \frac{L_s}{C_t} = R_s = 50\Omega \tag{2.36}$$

where L_s is the source inductor, and C_t is the total capacitance in source.

The quality factor of input circuit is expressed by Equation (2.37).

$$\mathrm{Q} = \frac{1}{(R_s + \mathrm{g}_m \frac{L_s}{C_t})\omega_0 C_t} = \frac{1}{2R_s\omega_0 C_t} \tag{2.37}$$

where ω_0 represents the resonance frequency of input matching network.

From Figure 2.3, output noises of noise sources at ω_0 are obtained as Equations (2.38)~(2.41).

$$i_{n,out,Rs} = \frac{g_m}{j2\omega_0 C_t} i_{n,Rs} \tag{2.38}$$

$$i_{n,out,Rout} = i_{n,Rout} \tag{2.39}$$

$$i_{n,out,d} = \frac{1}{2} i_{n,d} \tag{2.40}$$

$$i_{n,out,g} = \frac{g_m}{j\omega_0 C_t} \frac{jR_s\omega_0 C_t - 1}{j2R_s\omega_0 C_t} i_{n,g} \tag{2.41}$$

The correlation Equation (2.42) between $i_{n,g}$ and $i_{n,d}$ is suggested by [13]. c=-0.395j and its magnitude decreases for a long channel interface as the channel length falls down [26].

$$c = \frac{\overline{i_{n,g} \cdot i_{n,d}^*}}{\sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}}} \tag{2.42}$$

We can measure the PSD of output current due to $i_{n,g}$ and $i_{n,d}$ as calculated by Equations (2.43) and (2.44).

$$\begin{aligned} \overline{i_{n,out,g+d}^2} &= \overline{(Ai_{n,g} + Bi_{n,d})(Ai_{n,g} + Bi_{n,d})^*} \\ &= |A|^2 \overline{i_{n,g}^2} + |B|^2 \overline{i_{n,d}^2} + AB^* \overline{i_{n,g} \cdot i_{n,d}^*} + A^* B \overline{i_{n,g}^* \cdot i_{n,d}} \end{aligned} \tag{2.43}$$

$$\overline{i_{n,out,c}^2} = (jcAB^* - jcA^*B)\sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}} = \frac{g_m \cdot c}{2\omega_0 C_t} \sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}} \tag{2.44}$$

where, A and B are transfer functions for Equations (2.40) and (2.41), res pectively.

By using Equation (2.37), total noise factor for cascode topology at ω_0 is described as Equation (2.45).

$$F_{firs\ tstage} = \frac{\overline{i^2_{n,out,Rs}} + \overline{i^2_{n,out,d}} + \overline{i^2_{n,,out,g\cdot}} + \overline{i^2_{n,out,Rout}} + \overline{i^2_{n,,out,c}}}{\overline{i^2_{n,out,Rs}}} \tag{2.45}$$

It can be also rephrased as Equations (2.46)~(2.48).

$$F_{first\ stage} = 1 + \frac{\mathrm{g}_{g1}(Q^2 + \frac{1}{4})P^2 \quad \frac{\mathrm{g}_m^2}{\mathrm{g}_{dn}} + \gamma_1 \frac{\mathrm{g}_{dn}}{4} + \sqrt{\frac{\gamma_1 \mathrm{g}_{g1}}{4}} \; cP\mathrm{g}_m + \frac{1}{R_{out}}}{R_s Q^2 \mathrm{g}_m^2} \tag{2.46}$$

$$P = \frac{C_{gs}}{C_t} \tag{2.47}$$

$$\mathrm{g}_{dn} = \gamma \mathrm{g}_{d0} \tag{2.48}$$

The long-channel weights are 8/45 and 1 for g_{g1} and γ_1, respectively. Parameter P is always less than unity, since due to an extra capacitance (C_{ex}), C_t is always greater than C_{gs}.

The total noise factor of a LNA is defined as Equation (2.49) according to Friis equation.

$$F_{total} = F_{first-stage} + \frac{F_{subsequent} - 1}{G_F} \tag{2.49}$$

where, $F_{first\text{-}stage}$ is cascode topology noise factor, $F_{subsequent}$ is the noise factor of LNA, and G_F is the LNA gain of the first stage [27].

The dominant noise source of the LNA is the first stage noise due to high G_F. Therefore, the use of source inductive degeneration and the addition of L_x at the first stage reduce NF.

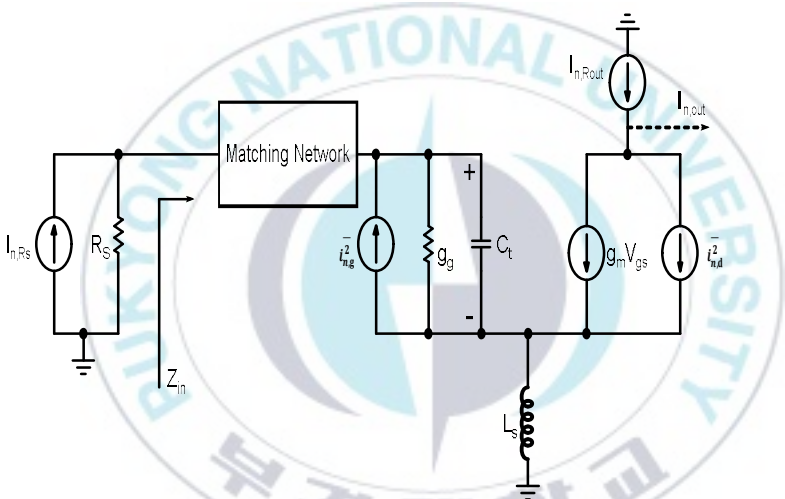


Figure 2.3. Small signal model of a cascode configuration including inductively degenerated noise sources.

2.5.4. Sensitivity

The sensitivity of the overall receiver is determined by the front-end noise figure. This relationship is provided analytically by Equation (2.50).

$$\text{Sensitivity(dBm)} = -174\,{}^{\text{dBm}}/_{Hz} + 10\log(\text{BW}) + NF_{tot} + 10\log(SNR_{out}) \quad (2.50)$$

where -*174dBm/Hz* characterizes the thermal noise at a temperature of 27°C, NF is the noise figure in *dB* of the cascaded stages of the whole system, *BW* is the noise bandwidth of the antenna, and the SNR_{out} is the minimum signal-to-noise ratio required by the detector to ensure an allowable level of the BER. The receiver noise floor N_{out} is equal to the sum of the first three terms of the equation below.

$$N_{out} = -174\,{}^{\text{dBm}}/_{Hz} + 10\log(\text{BW}) + NF_{tot}$$

Low *NF* of the LNA as evident from Equation (2.50), greatly decreases the sensitivity of the whole receiver.

2.6. Linearity

Dynamic range (DR) is commonly defined as the ratio of the highest possible input voltage without any noticeable distortion that can be tolerated by the circuit to the lowest input voltage that provides sufficient signal quality. Assuming that the LNA input signal is within the range of nanovolt (nV) or microvolt (μV), the LNA will have a large DR to ensure that it remains linear in the presence of large distortions. The amplifiers in the receiver chain must be able to minimize or cancel the adverse effects of large numbers of in-band interferences and inter-modulation/cross-

modulation induced by transmitter leakage or blockers at a high frequency. Nonlinear distortions including intermodulation, cross-modulation and signal distortion can be significant in high frequency amplifiers and restrict the upper DR band. Furthermore, in low frequency, the upper DR limit is usually defined as the input power that the circuit can manage without reaching the saturation region.

A wide in-band blocker is more likely to desensitize the circuit. It is measured by the 1-dB compression point (P_{1dB}). DR measures the efficiency of the signal constrained by the third-order input intercept point (*IIP3*). There are also plenty of linearity measurement methods for high frequency circuits, but perhaps the most obvious responses are the P_{1dB} and *IIP3*.

2.6.1. Compression Point 1-dB

The P_{1dB} is commonly defined as the input and output signal amplitude which causes essential gain to reduce by *1dB* from the ideal or normal small signal gain at the particular frequency as shown in Figure 2.4. Compression point on the LNA dynamic spectrum is known to be an upper limit. Thus input signals at the amplification point of out-of-band are typically compressed or saturated at the output.

It is possible to approximate a nonlinear system by using the Taylor

series defined in Equation (2.51).

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots \tag{2.51}$$

The compression point referred to input 1-dB in [28] can be determined as the Equation (2.52).

$$P_{1dB} = \sqrt{0.145 \left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.52}$$

where α_1 and α_3 are the first and third-order Taylor series expansion coefficients.

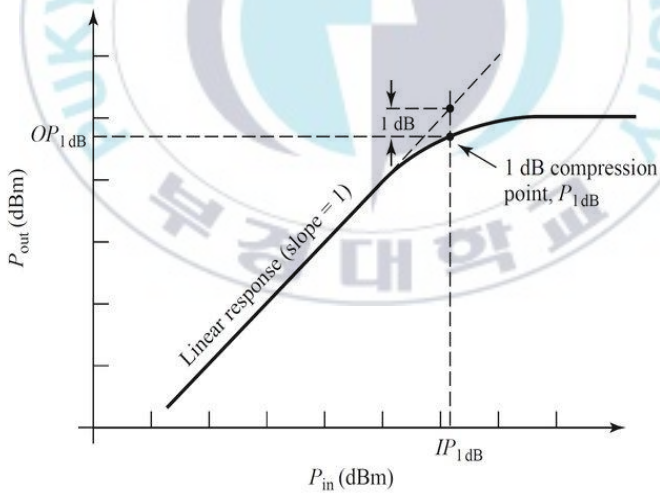


Figure 2.4. Definition of 1-dB compression point

2.6.2. Third-order Input Intercept Point (IIP3)

The multiplication of the input signal including its harmonics can cause

distortion with the nonlinear of the reasonable systems. The multiplication leads to the creation of terms of output called by intermodulation products (IMP). For instance, if two adjacent sinusoidal signals (also known as "two-tones") are fed to an LNA's nonlinear system input, due to the nonlinearity of the circuit, the mixing of the harmonics of these signals will produce the intermodulation products of the 2^{nd} and 3^{rd} order at the output but might hide the truth within the frequency response, thus reducing the desired output signal.

Consider a practical system with the input-output relation provided in Equation (2.51) to further investigate the effect of intermodulation. Let′s consider that the input signal has almost the same amplitude as Equation (2.53) but has two nearby sinusoidal components.

$$x(t) = A(\cos(\omega_1 t) + \cos(\omega_2 t)) \tag{2.53}$$

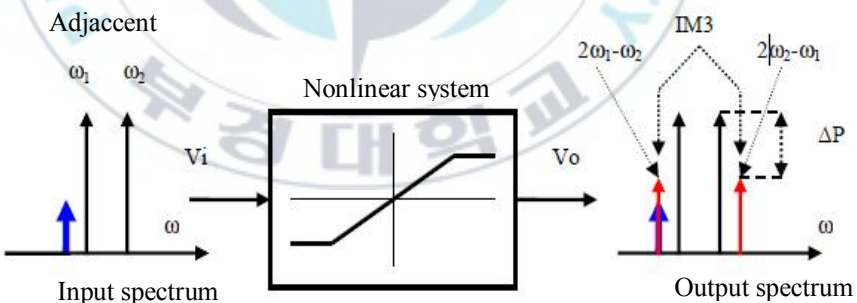
Then the following sentence defined in Equation (2.53) should appear at the output of the device. Equations (2.53) and (2.54) are found in the vicinity of both ω_1 and ω_2.

First

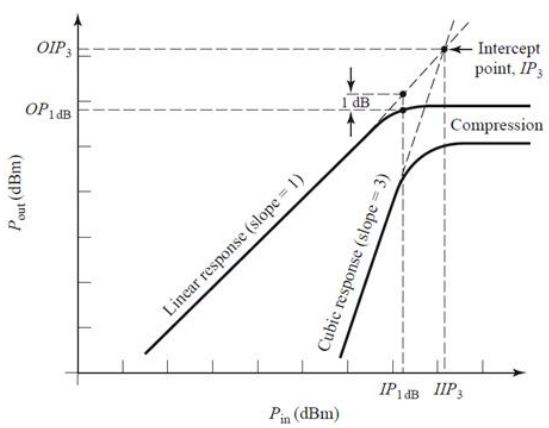
$$-\text{order terms:}\quad \begin{cases} at\ \ \omega_1 : y_{\omega_1} = \left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3\right)\cos(\omega_1 t) \\ at\ \ \omega_2 : y_{\omega_2} = \left(\alpha_1 A + \frac{9}{4}\alpha_3 A^3\right)\cos(\omega_2 t) \end{cases} \tag{2.54}$$

$$\text{Third}-\text{order IMP terms:}\quad \begin{cases} at\ \ 2\omega_1 - \omega_2 : y_{2\omega_1-\omega_2} = \left(\frac{3}{4}\alpha_3 A^3\right)\cos(2\omega_1 - \omega_2)t \\ at\ \ 2\omega_2 - \omega_1 : y_{2\omega_2-\omega_1} = \left(\frac{3}{4}\alpha_3 A^3\right)\cos(2\omega_1 - \omega_2)\,t \end{cases} \tag{2.55}$$

The input point which has the same output power as the fundamental signal and IMP is labeled in the third-order input intercept point as shown in Figure 2.5. It can be determined experimentally in Equation (2.56).



(a)



(b)

Figure 2.5. (a) Nonlinear system signal spectrum, and (b) conceptual description of *IIP3*

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.56}$$

These equations are valid if we presume that the $y_{\omega 1}$ and $y_{\omega 2}$ of Equation (2.55) are correct. Expressions $(\frac{9}{4}\alpha_3 A^3)$ are negligible. However, this principle no longer holds where the amplitude of signals is very high at the point of intercept. However, the measured IIP3 value in the Equation (2.56) is essentially an analysis of the weak input signal.

2.6.3. Consideration of System Level Linearity

A receiver chain typically consists of several cascaded blocks such as LNA, Mixer, VCO, etc. The overall linearity of a receiver chain therefore depends on the linearity and gain from each point. A receiver chain with different gain and *IIP3* of each individual block is given by the worst-case *IIP3* as the Equation (2.57) [29].

$$\frac{1}{A_{IIP3,tot}^2} = \frac{1}{A_{IIP3,1}^2} + \frac{\alpha_1^2}{A_{IIP3,2}^2} + \frac{\alpha_1^2\alpha_2^2}{A_{IIP3,3}^2} \tag{2.57}$$

where $A_{IIP3,i}$ and α_i are *IIP3* and gain of the *i*-th stage reward, respectively.

A thorough analysis of Equation (2.57) shows that if any stage of a cascade has a gain greater than unity, therefore the nonlinearity of the next stage becomes more critical [30]. This means that the nonlinearity of stages after LNA, e.g. mixer(s), has a major effect on the nonlinearity of LNA rather than the nonlinearity. As we know the LNA production increases, the *NF* decreases. Therefore the trait of linearity is in contrast with the *NF* situation, and there is a trade-off between linearity and *NF*. Usually designers are trying to optimize the LNA gain to obtain the best *NF*.

2.7. Input Impedance Matching Network

To transmit the antenna's maximum power to the LNA, the LNA's input port must be calibrated to the antenna's impedance, e.g., *50Ω*. For narrowband applications, the input impedance of LNA must be matched to antenna impedance in a single frequency with very narrow bandwidth. Even so, for wideband circuits, impedance matching at the LNA input port can be accomplished over a broad range of frequencies and is typically a major challenge given by the requirements for noise and power consumption.

The voltage standing wave ratio (VSWR) specified in Equation (2.58) is usually used to determine the coefficient of impedance matching [31].

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{2.58}$$

where Γ is the reflection coefficient as explained in Equation (2.59).

$$\Gamma = \left|\frac{Z - Z_0}{Z + Z_0}\right| \tag{2.59}$$

Z_o is the source characteristic impedance for this calculation that becomes usually equal to 50Ω, and Z is the real impedance of input. Perfect impedance matching with $Z=Z_o$ results in $\Gamma=0$ and $VSWR=1$. However, Γ must be less than $-10dB$ and the matching requirement are normally acceptable.

2.8. Circuit Design and Analysis

The rapid growth of wireless communications has pursued on low power, low cost, and high performance receivers [32]. In most cases, the millimeter wave circuits were considered by utilizing CMOS technology [33]. The main wireless receiver task is to detect the desired modulated signals [34]. Wireless receivers have to perform several functions such as tuning to the wanted signal carriers, filtering out the undesired signals, and amplifying the desired signal to compensate for power losses occurring during transmission, [35].

Thanks to growing speed of radar-based collision avoidance systems, vehicles can see the other objects including pedestrian and other vehicles, anticipate accidents and collision, control the braking system and steering wheel to save the people life, and reduce the severity of collisions. Radar transceivers are installed on the vehicles which operate in the all types of weather or sometimes both laser and camera are utilized to anticipate the imminent collision on the street or highways [36]. At first, collision avoidance systems search the surrounded area of the vehicles to detect the imminent crash. When the detection process is done, the system warns to the drivers by light, vibration in steering wheel or seat belt, and then the system based on the predefined distance fastens the seat belt and brakes, and finally controls the steering wheel to save the driver. The main frequency bands of radar applications are 24GHz and 77GHz. For the sake of detection of other near vehicles in the medium-short range and wide beam, 24GHz is mainstream [37]. The receiver for the automotive radar system operates in the band of 24 GHz frequency which is composed of LNA (low noise amplifier), down-conversion mixer, and VCO (voltage-controlled oscillator). The LNA is a crucial component for radio receivers [38], and it must meet several requirements such as good input matching, adequate gain and reasonably low noise figure to elevate received signal-to-noise ratio as well

as energy-efficiency for battery-powered portable devices [39].

This part presents low-power low-noise 24-GHz CMOS LNA for automotive collision avoidance radar. The proposed circuit is fabricated using 65nm RF CMOS technology and it is powered by 1.5V supply. To increase voltage gain, this circuit has cascode scheme, and it is optimized to decrease noise figure. Cascode inductive source degeneration technique is also utilized to match the circuit to source impedance.

2.8.1. Overview of 24GHz Radar

The automotive radar is the most promising and robust solution to vehicle sensing requirements in terms of environmental conditions, measurement capabilities, and ease of installation. The best frequency for this radar depends on the targeted application. In fact, this choice of frequency involves trade-off between several factors such as transmitted and received powers. The systems consist of three types such as short range radar (SRR), medium-short range (MRR) and long range radar (LRR). The CMOS-based 24-GHz SRR sensors with distance up to approximately 30 meters are under development for a variety of further applications [40]. The SRR may cover many applications such as parking aid, ACC with stop and go, pre-crash or collision warning, back-up function, etc. Since it has also

better performance in azimuth angle and in range measurements, it is suitable for automotive applications providing parking aid, pre-crash detection, side object detection and blind spot detection [41].

2.8.2. Design of the Proposed 24GHz CMOS LNA

Figure. 2.6 shows the proposed low-power low noise-noise 24-GHz CMOS LNA. This LNA is implemented using the 65nm RF CMOS process. This process has been retained because of its good low noise performance, the unity current gain cut-off frequency (f_T) of 120GHz and the maximum oscillation frequency (f_{max}) of 140GHz.

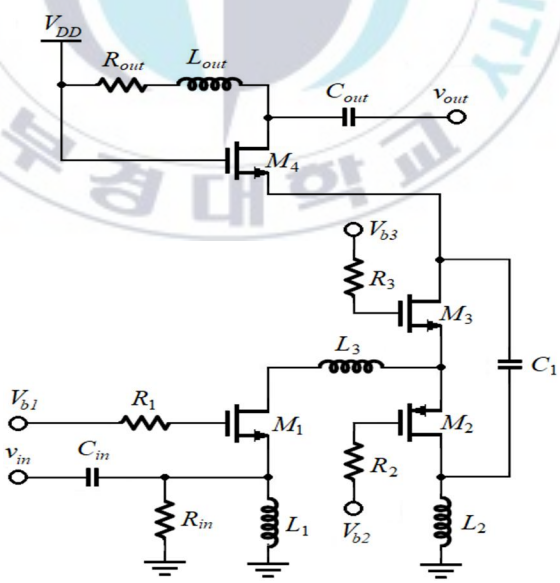


Figure 2.6. 24GHz CMOS LNA

Successful integration of the LNA at 24GHz depends on minimizing parasitic capacitances and losses to maintain adequate gain, designing with low voltage swing for low breakdown devices, and achieving sufficient linearity required for low spectrally efficient and variable envelope modulation scheme.

Providing a resistive input impedance of 50Ω is a critical requirement of an LNA. The 50Ω termination is required mainly by the previously band select filter L_3 with parasitic capacitance and transistor M_1 is biased by adding parasitic capacitance to the input impedance matching. The third-order non-linear transconductance coefficient g_{m3} is performed by gate-drain and gate-source capacitances of basic components, and it reduces linearity performance. To improve noise figure and linearity, we propose a CG (common gate) NMOS-PMOS inverter scheme for the cascode LNA as a linearizer. The proposed linearization method accepts NMOS and PMOS transistors into common gate configuration with the second-order and third-order nonlinearity to improve the linearity performance [42], [43].

To reach very low third-order distortion and low power, it is very important to reduce the second-order and third-order nonlinearities. It is very important to minimize or cancel g_{m2} and g_{m3} to decrease the third-order intermodulation distortion and to improve *IIP3* (third-order input intercept

point). The inductor L_2, and the parasitic capacitances at the drain of M_2 and M_4 form provide broadband network.

Let's consider drain current I_{dtotal} of M_1 through the M_2 and M_3 transistors as shown in Fig. 2.7. For M_4, $V_{g4} = V_{dd}$, $V_{s4} = V_{d3}$, $I_{d4} = (V_{dd}-V_{d4})/R_{out}$, $I_{d4} = I_{d3}$ and $I_{d4} = 0$, since M_1 is connected to the ground through capacitor C_1 for $I_{d1} = 0$. From KCL, $I_{s3} = I_{d1} + I_{s2}$, $I_{s2} = I_{s3}$, $V_{dd}-I_{d4}R_{out}-V_{ds4}-V_{ds3} = V_{ds2}$, and $V_{dd} = I_{d4}R_{out} + V_{d4}$, and we obtain Equations (2.60)~(2.62).

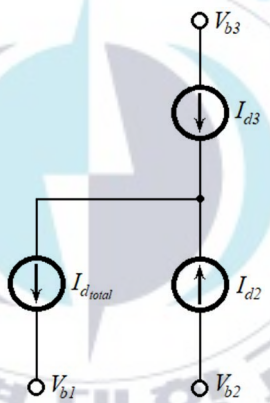


Figure 2.7. Ideal view of the inverter stage

$$I_{d2} = g_{m1_2}V_{gs_2} + g_{m2_2}V_{gs_2}^2 + g_{m3_2}V_{gs_2}^3 \tag{2.60}$$

$$I_{d3} = g_{m1_3}(-V_{gs_3}) + g_{m2_3}(-V_{gs_3})^2 + g_{m2_3}(-V_{gs_3})^3 \tag{2.61}$$

$$I_{d_{total}}(V_1) = I_{d2} + I_{d3}$$
$$= \left(g_{m1_2}V_{gs_2} + g_{m2_2}V_{gs_2}^2 + g_{m3_2}V_{gs_2}^3\right) - \left(g_{m1_3}(-V_{gs_3}) + g_{m2_3}(-V_{gs_3})^2 + g_{m2_3}(-V_{gs_3})^3\right) \tag{2.62}$$

Since V_{gs_3} is a function of V_{gs_2}, it is expressed to power series of V_{gs_2} as follows:

$$V_{gs3} = c_1 V_{gs_2} + c_2 V_{gs_2}^2 + c_1 V_{gs_2}^3 \tag{2.63}$$

where $c_i s$ are in general frequency dependent. In practice, the π-network cancels the effects of c_2 and c_3 at the frequency of interest. To find the coefficient $c_i s$, we should solve the equation after expanding I_{dtotal} as a power series of V_{gs2} and replacing it with Equation (2.63) we obtain Equation (2.64) [45].

$$\begin{aligned} &= I_{d2} + I_{d3} \\ &\cong \left(g_{m1_3} + c_1 g_{m2_2}\right) V_{b3} + \left(g_{m2_3} + c_1^2 g_{m2_2}\right) V_{b3}^2 + \left(g_{m3_3} + c_1^3 g_{m3_2}\right) V_{b3}^3 \cdots \end{aligned} \tag{2.64}$$

where g_{m1}, g_{m2} and g_{m3} are the main transconductance, second-order and third-order nonlinearity coefficients respectively [20]. The second order nonlinearity is canceled in output due out off phase signal by NMOS and PMOS. The optimum biasing is used to obtain a high *IIP3* by reducing the total g_3, the *IIP3* can be calculated as follows: [46].

$$A_{\mathrm{IIP3}} = \sqrt{\frac{3}{4}\left|\frac{g_{m1}}{g_{m3}}\right|} \tag{2.65}$$

The $g_{m3,d3}$ changes from positive to negative when the transistor moves from weak to strong inversion region. In other words, by changing gate bias voltage of PMOS transistor, the parameter C_1 can be varied. It can be deduced from Equation (2.65).

2.8.3. Small Signal Analysis

In LNA solutions it is significant that the input impedance is matched with the antenna impedance to carry out effective power transfer. LNA is proposed like a high frequency application and must be terminated by inherent 50Ω impedance. If there is any essential turning of load impedance from 50Ω seen by the filter, then there can be a loss and wave at pass band and stop band characteristics of the filter. Figure 2.8 shows simplified high-frequency small signal model of cascade topology with inductively degenerated for the LNA. μ_p and μ_n are mobility of charge carriers of PMOS and NMOS transistors respectively. *W, L,* and C_{ox} represent the transistor's width, length, and gate capacitance per unit area.

By applying the KCL at source node we get

$$C_{gs} = C_{gd} = \frac{C_{ox}WL}{2} = C_{gc} \ (V_s = V_d). \tag{2.66}$$

where *W* and *L* represent the transistor's width and length, respectively, and C_{ox} is gate capacitance per unit area.

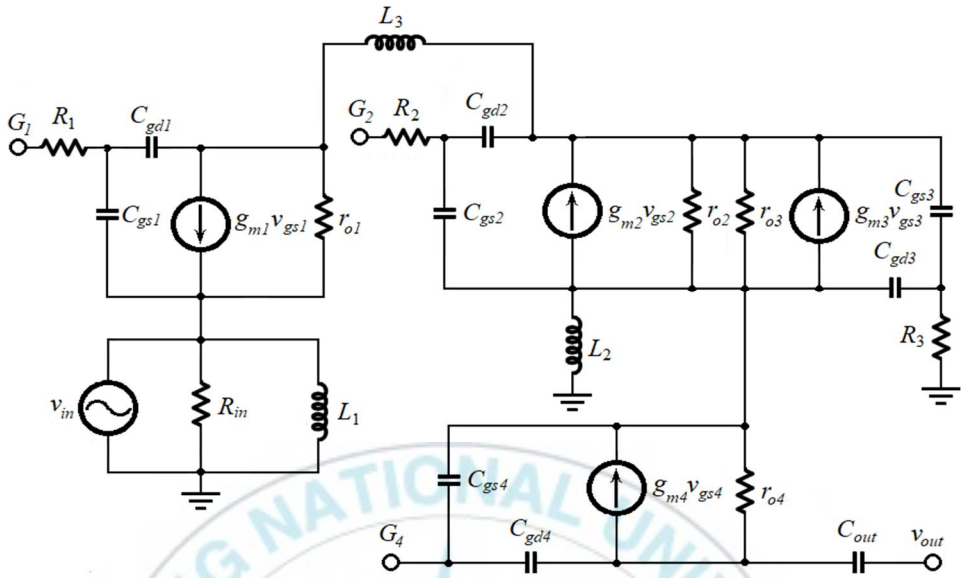


Figure 2.8 High-frequency small signal models for the LNA.

By applying the KCL at drain node d_1 of M_1, we get Equations (2.67)~(2.72).

$$(V_{d1} - V_{g1})\text{jw}C_{gd1} + g_{m1}V_{gs1} + \frac{(V_{d1} - V_{s1})}{r_0} + \frac{(V_{d1} - V_{s2})}{jwL_3} = 0 \tag{2.67}$$

$$(V_{d1} - V_{g1})\text{jw}C_{gd1} + g_{m1}V_{gs1} + \frac{V_{ds1}}{r_0} + \frac{(V_{d1} - V_{s2})}{jwL_3} = 0 \tag{2.68}$$

$$(V_{d1} - V_{g1})(-\text{w}^2 L_3 C_{gd1})r_0 + jwL_3 r_0 g_{m1}V_{gs1} + jwL_3 V_{ds1} + r_0(V_{d1} - V_{s2}) = 0 \tag{2.69}$$

$$V_{d1}[-w^2 L_3 r_0 C_{gd1} + r_0] + V_{g1}w^2 L_3 r_0 C_{gd1} - r_0 V_{s2} + jwL_3 V_{ds1} + jwL_3 r_0 g_{m1}V_{gs1} = 0 \tag{2.70}$$

$$V_{d1}\left[-w^2L_3r_0C_{gd1}+r_0\right]+V_{g1}w^2L_3r_0C_{gd1}-r_0V_{s2}+jwL_3V_{d1}$$
$$-jwL_3V_{s1}+jwL_3r_0g_{m1}V_{g1}-jwL_3r_0g_{m1}V_{s1}=0 \quad (2.71)$$

$$V_{d1}\left[-w^2L_3r_0C_{gd1}+r_0+jwL_3\right]+V_{g1}\left[w^2L_3r_0C_{gd1}+jwL_3r_0g_{m1}\right]+$$
$$V_{s1}[-jwL_3-jwL_3r_0g_{m1}]-r_0V_{s2}=0 \quad (2.72)$$

Now let's analyze the input impedance of the cascade topology using inductive source degeneration technique will explain with the circuit shown in Figure 2.8. The transistor M_1 is replaced with a high-frequency small-signal model consisting of gate-source capacitor C_{gs1}, gate-drain capacitor C_{gd1}, transconductance g_{m1}, and source degeneration inductor L_1. The input impedance matching is a core technology in RF circuit design. As seen in the Figure 2.6 the input impedance of transistor M_1 is a series an LC circuit given by equation (2.81).

The noise performance of the design sample is good after impedance matching is done.

By applying the KCL at source node s_1 we also obtain Equations (2.73)~(2.75).

$$I_{in}=V_{s1}(\frac{1}{R_{in}}+\frac{1}{jwL_1})-g_{m1}V_{gs1}-V_{ds1}(\frac{1}{r_0}+jw(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}) \quad (2.73)$$

$$I_{in} = \frac{V_{s1}}{R_{in}} + \frac{V_{s1}}{jwL_1} - g_{m1}V_{gs1} - \frac{V_{ds1}}{r_0} - V_{ds1}jw(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}) \quad (2.74)$$

$$I_{in} = V_{s1}\left(\frac{1}{R_{in}} + \frac{1}{jwL_1} + g_{m1} + \frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}\right)\right)$$

$$-g_{m1}V_{g1} - V_{d1}\left(\frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}\right)\right) \quad (2.75)$$

For AC analysis, C_{in} can be shorted, and by neglecting the term V_{d1} and V_{g1}, and using Equations (2.73)~(2.75), we obtain Equations (2.76) and (2.77). $V_{in} = V_{s1}$ by inserting this value and rearranging, so the input impedance Z_{in} is expressed by Equations (2.78) and (2.79).

$$I_{in} = V_{in}\left(\frac{1}{R_{in}} + \frac{1}{jwL_1} + g_{m1} + \frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}\right)\right) \quad (2.76)$$

$$\frac{V_{in}}{I_{in}} = Z_{in} \ (\Omega) \quad (2.77)$$

$$Z_{in} = \frac{1}{\left(\frac{1}{R_{in}} + \frac{1}{jwL_1} + g_{m1} + \frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}\right)\right)} \quad (\Omega) \quad (2.78)$$

where Z_{in} and output impedance Z_{out} of each stage are optimized at 24GHz.

$$Z_{in} = R_{in}//X_{L1}//\frac{1}{g_{m1}}//r_0//X_C \tag{2.79}$$

where $X_{L1} = jwL_1$ and $X_C = \frac{1}{jw(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}})}$.

By assuming r_0=∞, we get the simplified form of Z_{in} as shown below:

$$Z_{in} = R_{in}//X_{L1}//\frac{1}{g_{m1}}//X_C \tag{2.80}$$

On deactivating the input source V_{in} and applying KCL at the output node, we can get output impedance Z_{out}. At the input node s_1, we also obtain Equations (2.81) and (2.82).

$$I_{s1} = g_{m1}V_{gs1} + \frac{V_{ds1}}{r_0} + V_{ds1}jw(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}) \tag{2.81}$$

$$V_{s1} = I_{s1}\left[\frac{R_{in}jwL_1}{R_{in}+jwL_1}\right] \tag{2.82}$$

By applying KCL at the output node d_4, inserting $V_{d4} = V_{out}$, and rearranging, we get Equations (2.83)~(2.87).

$$\frac{V_{out}-V_{s4}}{r_0} + g_{m4}V_{gs4} + \left[\left(\frac{R_{out}+jwL_{out}\frac{1}{jwC_{gd4}}}{R_{out}+jwL_{out}+\frac{1}{jwC_{gd4}}}\right)+\frac{1}{jwC_{gs4}}\right](V_{out}-V_{s4}) \tag{2.83}$$

$$\frac{V_{out}}{r_0} + V_{out}\left[\left(\frac{R_{out} + jwL_{out}\frac{1}{jwC_{gd4}}}{R_{out} + jwL_{out} + \frac{1}{jwC_{gd4}}}\right) + \frac{1}{jwC_{gs4}}\right] = I_{out} \tag{2.84}$$

$$Z_{out} = \left[\frac{1}{r_0} + \frac{R_{out} + jwL_{out}}{jwC_{gd4}(R_{out} + jwL_{out}) + 1} + \frac{1}{jwC_{gs4}}\right]^{-1} (\Omega) \tag{2.85}$$

$$Z_{out} = \left[\frac{1}{r_0} + \frac{1}{jwC_{gd4} + G_{out}} + \frac{1}{jwC_{gs4}}\right]^{-1} \tag{2.86}$$

where $G_{out} = \frac{1}{R_{out} + jwL_{out}}$, by assuming r_0=∞, we obtained the simplified form of Z_{out} as shown below:

$$Z_{out} = \frac{jwC_{gs4}(jwC_{gd4} + G_{out})}{jw(C_{gd4} + C_{gs4}) + G_{out}} \tag{2.87}$$

Now let's get voltage gain. From the voltage and current of transistors M_1, M_2, M_3 and M_4, we also obtain Equations (2.88)~(2.96).

$$V_{s2} = V_{d1} - I_{d1,d2}jwL_3 \tag{2.88}$$

$$V_{d1} = I_{ds1}r_{01} + V_{s1}; \tag{2.89}$$

$$V_{d4} = I_{ds4}r_{04} + V_{s4} = V_{out} \tag{2.90}$$

As $V_{s1} = V_{in}$ for transistor M_1 we get Equation (2.91).

$$V_{d1} = I_{ds1}r_{01} + V_{in} \tag{2.91}$$

By rearranging Equations (2.88) and (2.90), we get Equation (2.92).

$$V_{s2} = I_{ds1}r_{01} + V_{in} - I_{d1,d2}jwL_3 \tag{2.92}$$

As $V_{s2} = V_{s3}$ for transistor M_2 and M_3, we get Equation (2.93).

$$V_{s3} = I_{ds1}r_{01} + V_{in} - I_{d1,d2}jwL_3 \tag{2.93}$$

As shown in Figure 2.8 we will get Equation (2.94).

$$V_{d3} = I_{ds3}r_{03} + V_{s3} \tag{2.94}$$

By rearranging Equations (2.93) and (2.94), we get Equation (2.95).

$$V_{d3} = I_{ds3}r_{03} + I_{ds1}r_{01} + V_{in} - I_{d1,d2}jwL_3 \tag{2.95}$$

As $V_{d3} = V_{s4}$ for transistor M_3 and M_4, we get Equation (2.96).

$$V_{s4} = I_{ds3}r_{03} + I_{ds1}r_{01} + V_{in} - I_{d1,d2}jwL_3 \tag{2.96}$$

By rearranging Equations (2.90) and (2.96), we get Equation (2.97).

$$V_{out} = I_{ds1}r_{01} + V_{in} - I_{d1,d2}jwL_3 \quad + I_{ds3}r_{03} + I_{ds4}r_{04} \tag{2.97}$$

The gain of the proposed LNA should be as large as possible to reduce the noise figure. And the voltage gain of proposed LNA is shown in Equation (2.104).

As shown in Figure 2.8 we can calculate A_v voltage gain.

$$A_{v1} = g_{m1}(R_{D1}//r_{01}) \tag{2.98}$$

Where $R_{D1} = (jwL_3//r_{02})$ represent the series resistance of L_3

$$A_{v1} = g_{m1}(jwL_3//r_{02}//r_{01}) \tag{2.99}$$

$$A_{v3} = g_{m3}(r_{03}//\frac{1}{g_{m4}}//r_{04}) \tag{2.100}$$

$$A_{v4} = g_{m4}(r_{04}//R_{out} + jwL_{out}) \tag{2.101}$$

$$A_v = g_{m1}(jwL_3//r_{02}//r_{01})\ \ g_{m3}(r_{03}//\frac{1}{g_{m4}}//r_{04})g_{m4}(r_{04}//R_{out} + jwL_{out}) \tag{2.102}$$

$$A_v = g_{m1}g_{m3}g_{m4}((jwL_3//r_{02}//r_{01})\ \ (r_{03}//\frac{1}{g_{m4}}//r_{04})(r_{04}//R_{out} + jwL_{out})) \tag{2.103}$$

If we assumed that $r_{01} = r_{02} = r_{03} = r_{04} = r_0$ are same

$$A_v$$

$$= g_{m1}g_{m3}g_{m4}\left(\frac{jwL_3r_0}{2jwL_3 + r_0}\right)\left(\frac{r_0}{2 + r_0g_{m4}}\right)(r_0//R_{out} + jwL_{out}) \tag{2.104}$$

By assuming $r_0=\infty$, therefore we get Eq. (2.105).

$$A_v = g_{m1}g_{m3}g_{m4}(R_{out} + jwL_{out}) \lim_{r_0\to\infty}\left(\frac{jwL_3r_0}{2jwL_3 + r_0}\right) \lim_{r_0\to\infty}\left(\frac{r_0}{2 + r_0g_{m4}}\right) \tag{2.105}$$

After solving the above Eq. (2.105), can be further simplified as follows

$$A_v = g_{m1}g_{m3}g_{m4}(R_{out} + jwL_{out})\frac{jwL_3}{g_{m4}} \tag{2.106}$$

$$A_v = G_T(R_{out} + X_{Lout})(X_{L3}) \tag{2.107}$$

where $X_{Lout} = jwL_{out}$, $X_{L3} = jwL_3$ and $G_T = g_{m1}g_{m3}$

Throughout the amplification phase the noise figure *(NF)* in LNA specifies the intrinsic LNA noise applied to the desired or desirable signal.

NF is a method of source admittance that looks through the two-port network input terminal. To achieve the NF_{min}, an optimum admittance, namely Y_{opt}, should be introduced to the network. The expressions for NF_{min} and Y_{opt} can be derived for a MOS device by considering a two-port network

model for the MOS device. The gate-source terminal in this configuration is the port of input, and the terminal drain-source is the port of output.

2.8.4. Implementation

The design plays a very major part in deciding the output of the chip produced in an RF circuit. The main factors to be considered in the RF layout are system matching and symmetry, parasites, current density in interconnections, thermal variations and substrate effects [47]. For some significant factors for RF layout, a thicker nanowire layer should be used to realize chip capacitors, and on-chip supply decoupling should be used to reduce high frequency noise of the power supply. In sensitive circuit areas physical structural element can also be used to avoid parasites.

The Cadence software program is used to provide layout and post-processing of LNA. The circuits are designed and fabricated using 65nm RF CMOS technology. This technology offers six metal layers with two top layers of 0.6μm thick copper. Shield pads for inductors are employed at each port. Figure 2.9 and Figure 2.10 show layout and die photograph of the proposed LNA. Grounded metal underneath the pads prevents loss of the signal power and noise generation associated with the substrate resistance. Ground rings are placed around each transistor at minimum distance to

reduce the substrate loss. To minimize parasitic capacitance all transistors are designed by folded structure [48]. Signal lines are wide enough to meet electro-migration requirements. Ground lines were made wide to provide low impedance paths.

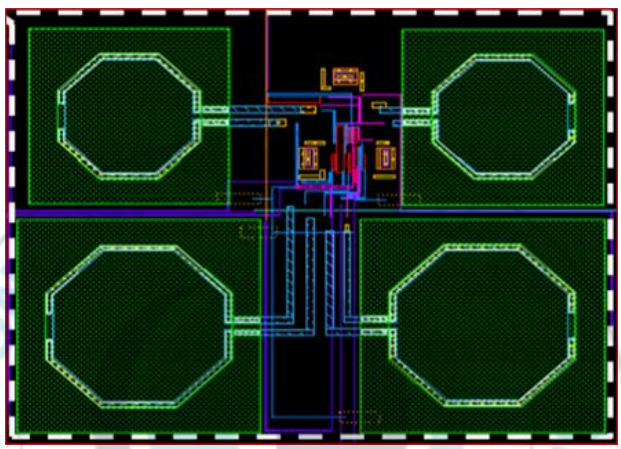


Figure 2.9. Layout of the 24 GHz LNA

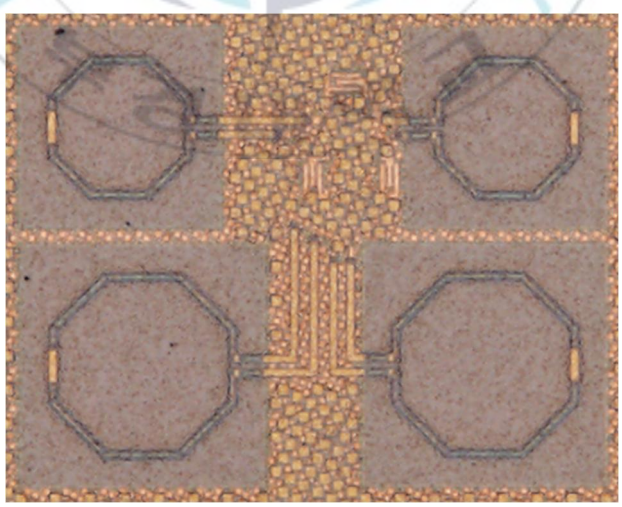


Figure 2.10. Die photograph of the proposed LNA

The decoupling capacitor is added to bypass high frequency noise from the bias voltage. Grounded guard ring with substrate connection surrounds the inductor to minimize substrate noise. The MIM capacitors are used for high quality factors and the resistors of tantalum-nitride thin film are used. Large on-chip bypass capacitors are placed between each V_{DD} and ground. The die occupies 0.60×0.60mm^2 including pads and 0.31×0.35mm^2 without pads.

2.9. Measurement Results and Discussions

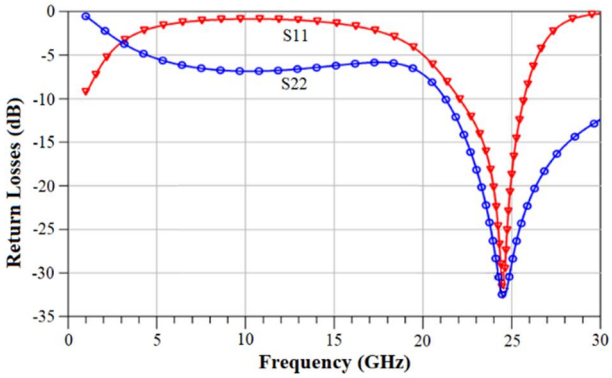
2.9.1. Measurement of S-Parameter and Noise Figure

The input and output pads are laid out in GSG configuration with a pitch of 50μm to perform wafer level testing for LNA using a probe station with network analyzer. We performed 2-port measurements. The measurements are based on a separate LNA test chip. The power of −20dBm is applied from the synthesized sources at both port 1 and port 2. We applied the attenuators of 0dB at both port 1 and port 2.

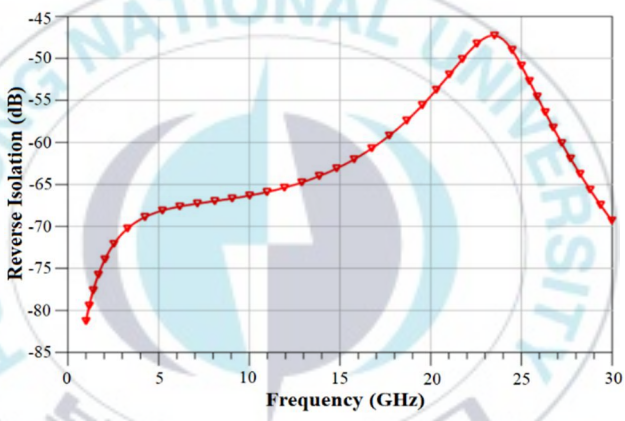
Obviously, downscaling of CMOS technologies has significant impact on the design of analog and radio frequency circuits. Particularly, in low supply voltage circuits, as the technology downscales, the available voltage headroom decreases, and so it makes the design procedure difficult.

Additionally, since the voltage headroom is smaller, the low power consumption in wireless and electronic portable devices and applications is becoming more important. In analog and RF blocks, high output power with high efficiency is desirable, but with the above-mentioned limitations on the recent technologies, achieving these goals requires special attention on the designing circuits with new techniques and topologies. From Figure 2.6 and Figure 2.7, the proposed LNA showed total dc current of 3.825mA at 1.5V supply, so we obtained the lowest power consumption of 4.59mW as compared to conventional results [49], [50].

Figure 2.11(a) and (b) show input and output return losses (S_{11}, S_{22}) and reverse isolation (S_{12}), respectively. Input and output impedance matching is so important to obtain low input and output return losses. Ideal input and output impedances of the amplifier must have 45~50Ω at the operation frequency. As shown in Figure 2.11, the LNA showed very low input return loss of -32.8dB, very low output return loss of -32.7dB, and very low reverse isolation of -47dB as compared to conventional results [52].



(a) Input and output return losses, S_{11} and S_{22}.



(b) reverse isolation (S_{12})

Figure 2.11. S-parameter for the proposed LNA.

Voltage gain is very important parameter in GHz-band LNA. Figure 2.12 shows voltage gain (S_{21}). As shown in Figure 2.12, the proposed LNA showed very high voltage gain of 24.3dB at the operation frequency of 24GHz as compared to conventional results [53], [54].

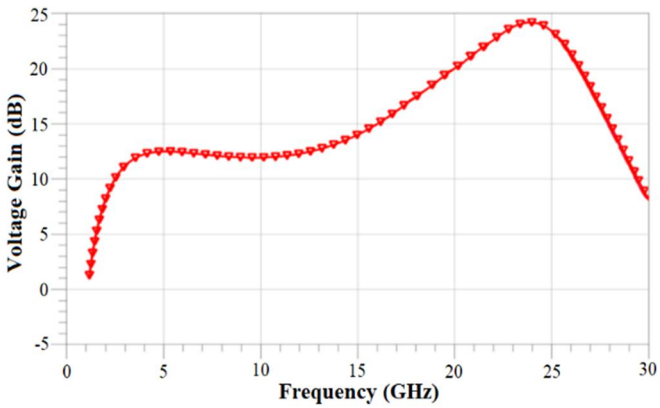


Figure 2.12. Voltage gain (S_{21}).

Figure 2.13 shows noise figure. Noise figure is measurement factor of degradation of signal-to-noise ratio (SNR) as the incoming signal from antenna traverses the receiver front-end. Mathematically, noise figure is defined as the ratio of the input SNR to the output SNR of the system. As shown in Figure 2.13, the proposed LNA showed very low noise figure of 2.98dB as compared to conventional results [55], [56].

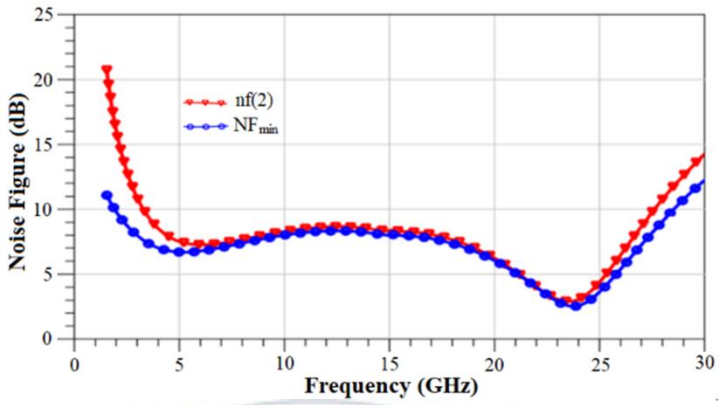


Figure 2.13 Noise Figure

2.9.2. IIP3 and Stability Factor

Figure 2.6 in previous session showed that the proposed common gate NMOS/PMOS technique inverted in between the input and output port of LNA & due to the inclusion of C_{in} & C_1 the linearity increase.

From the figure 2.14 it can be observe that, to achieve high linearity or to achieve the low *IIP3* distortion g_{m2} and g_{m3} should be reduced or minimized. The inclusion of inductor with proper size cancels the parasitic capacitive effects which results in an effective short circuit over a complete bandwidth. Under this condition, non-linearity of M_2 can be neglected. The non-linearity drain current of M_1 moves toward the M_2 and M_3 transistors which are utilized as CG configuration, and as a current buffer. The main responsibility of stage (M_2 and M_3) is to absorb non-linearity of M_1 drain

current. Thus, the fundamental current component of M_1 can be delivered to output port. The inclusion of capacitor C_1 is inserted between drain of M_3 and M_2 to equalize the voltage levels at the drains of M_3 and M_2. The IIP3 of the LNA is 3.2dBm.

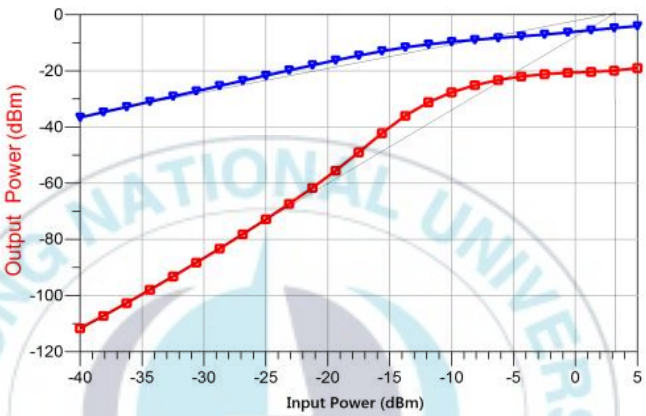


Figure 2.14. IIP3 of the LNA

Among all the main performance parameters, if the circuit works as planned without unnecessary oscillations that could virtually destroy the active devices caused by voltage overload, the LNA's stability is a fundamental requirement. The K and $|\Delta|$ are the common parameters for calculating the stability of the circuit. K and $|\Delta|$ values are derived from Equations (2.22)~(2.23). Since the K is greater than unity, and so the LNA is stable at the desired frequency as shown in Figure 2.15. The stability factor of the K is approximately 8.5 at 24 GHz.

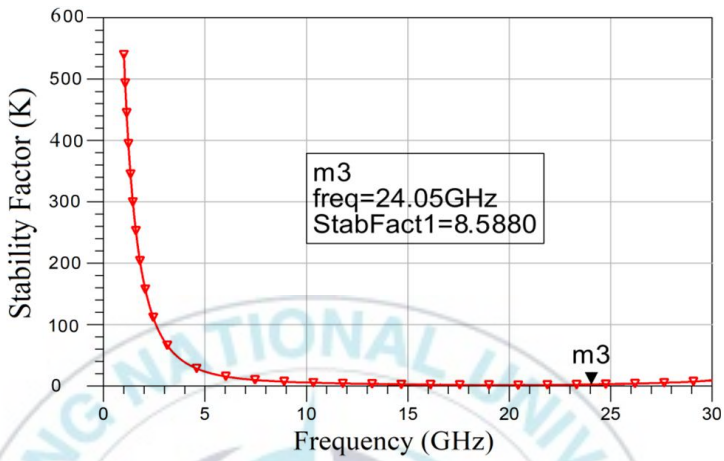
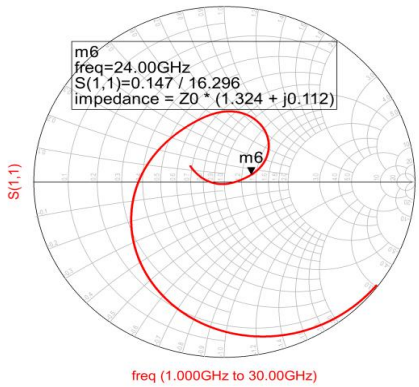
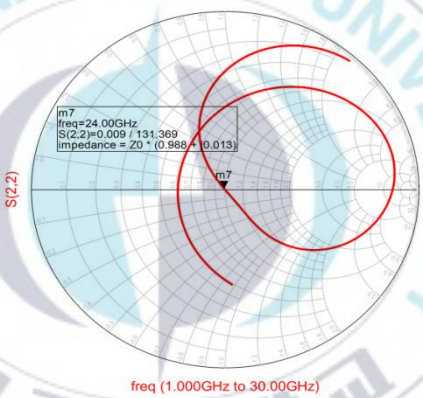


Figure 2.15. Stability factor of the LNA

In addition, the cascode LNA is operationally feasible since its frequency for input and output impedance is not flicked to the outer edge of the Smith chart as shown in Figure 2.16. This simulation result verifies to input and output impedance matching that the proposed LNA has input impedance of approximately 65Ω and the output impedance of approximately 49Ω at the operating frequency 24GHz.



(a) Input impedance matching



(b) Output impedance matching

Figure 2.16. Smith chart simulation

The performance summary of the proposed LNA is compared in Table 2.1. As can be seen from Table 2.1, the proposed LNA showed the lowest power consumption of 4.59mW, the highest voltage gain of 24.3dB, and the

lowest noise figure of 2.98dB as compared to conventional results [57], [58], [59], [60]. It also has the smallest die size 0.31×0.35mm^2 without pads as compared to recently reported research results.

Table 2.1. Comparison summary for recently reported research results

Parameters	This Work	[57]	[58]	[59]	[60]
Frequency (GHz)	24	24	24	24	24
Technology (nm)	CMOS 65	CMOS 103	CMOS 180	CMOS 180	BiCMOS 170
Supply voltage (V)	1.5	1.2	1	-	1.2
S_{21} (dB)	**24.3**	-	13.1	18.19	22.5
S_{11}/S_{22} (dB)	**-32.8/-32.7**	-9.5	-18	-25	-12/-13
Power (mW)	**4.59**	15	14	11.3	42
IIP3 (dBm)	**3.2**	-	0.54	-16.5	-15.5
Noise Figure (dB)	**2.98**	3.8	3.9	5.8	3.2
Die area (mm^2)	**0.31×0.35**	1.7×1.2	0.57×0.6	0.94×0.5	2.2×0.9

2.10. Summary

In this paper, we proposed low-power low-noise 24-GHz CMOS LNA for automotive collision avoidance radar. This circuit is implemented in 65nm RF CMOS process. To increase voltage gain and decrease power consumption, we utilized cascode inductive source degeneration technique. The LNA was optimized by minimization of the inherent LNA noise added to the desired or wanted signal during the process of amplification to reduce noise figure. The proposed LNA showed total dc current of 3.825mA at 1.5V supply, so we obtained the lowest power consumption of 4.59mW as compared to conventional results. It also showed the lowest noise figure of 2.98dB, high voltage gain of 24.3dB, good S-parameter results and small die size $0.31 \times 0.35 mm^2$ without pads as compared to recently reported research results.

Chapter 3

3. The Design of Low-Power Down-Conversion Mixer for 24 GHz Automotive Radar

3.1 Background

The mixer is an essential module in any telecommunication system whose impact is critical on the performance of all functions. All in all to restore the desired signal, we are obliged to accomplish a frequency conversion by a mixer allowing a temporal multiplication of two signals, one RF coming from a receiving antenna possibly filtered and amplified and the other LO coming from of a local oscillator as shown in Figure 3.1, the result is a transposition to a high or low intermediate frequency (IF) free of interference. However a set of difficulties arise from this process which induces a challenge in terms of gain, noise, linearity, insulation, consumption and cost Eqs. (3.1).

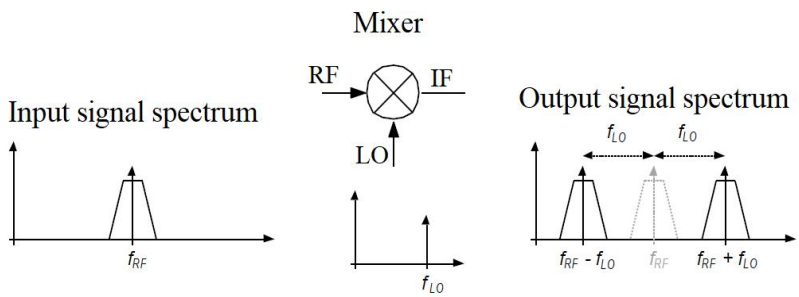


Figure 3.1 Block diagram of frequency conversion

An ideal mixer is an analog multiplier with three ports as shown in Figure 3.2. In practice the mixing operation is performed using non-linear components, although the multiplication operation is mathematically simple, it turns out to be almost difficult “if not impossible” to perform in an ideal way Eqs. (3.2). In addition, as shown in the assembly diagram in Figure 3.1, the mixer is located as an interface in any receiver unit between an LNA (low noise amplifier) receiving the RF signal and a filter ensuring the reception of the signal in the baseband desired. As a result, the choice of CMOS technology adopted for the mixer is essential to ensure, on the one hand, a good gain for the entire system and an excellent impedance match between the input and the output of the mixer, unlike the technologies GaAs or SiGe which are more expensive.

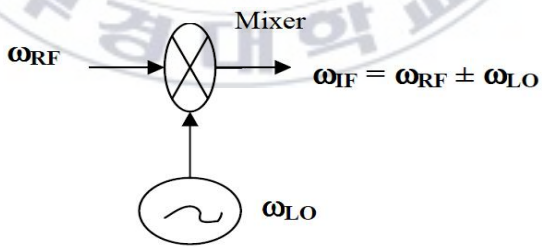


Figure 3.2 Block diagram of a frequency mixer

Theoretically, the mixer generates an IF output whose frequency is equal to the sum and the difference of the RF and LO input signals, expressed by the relation:

$$(A\cos\omega_{RF}t)(B\cos\omega_{LO}t = \frac{AB}{2}[\cos(\omega_{RF} - \omega_{LO})\,t + \cos(\omega_{RF} + \omega_{LO})\,t] \quad (3.1)$$

This result allows us to show that a temporary multiplication of signals leads to an addition or a difference in frequency. This is why the mixer has the advantage of performing a frequency conversion. Really, the behavior of the mixer is not ideal, it causes nonlinear distortion, as illustrated in Figure 3.3 translated by the generation of other harmonics different from the useful signal, and the most harmful are the intermodulation frequencies. There are two distinct topologies of mixers: passive and active.

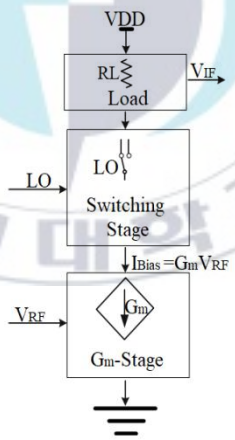


Figure 3.3 Specific concept of active mixing

Study and definition of passive mixers are beyond focus in this chapter and will be discussed only for the active mixers. Due to their reasonable

conversion gain, noise figure, and linearity, Gilbert-type mixers have recently become widely used. Note that since mixers are the second block in the receiver chain, the main characteristics are linearity, conversion gain, and power consumption.

However according Friis equation, LNA's noise figure is much more significant than mixer because LNA's gain is usually higher that mostly leads to the suppression of frontend noise. In cascode architecture, Gilbert cell is basically stacked at the top of the Gm-stage. As a result, Gilbert-type isn't a good choice in low supply voltage, low voltage headroom and low power mixer circuits.

A few techniques were proposed to operate in low power supply and low power consumption for the mixers. Another method consisted of biasing the transistors in the region of weak inversion (subthreshold). In [34], the topology of subthreshold, the ratio of transconducatnce (g_m) to drain current (I_d) is very high due to the fact that drain current is very low and can be presumed to be in the μA range.

As mentioned previously, the Gilbert cell configures in cascode configuration that increases the voltage supply and headroom supply. The bias offset technique has been suggested to solve this problem [35].

3.2 Linearity Methods

The linearity of a system determines the maximum allowable level of the signal at its input. Really, not every device is perfectly linear it does indeed exhibit a certain degree of non-linearity. Thus, its transfer function is not perfectly linear as shown in Figure 3.4. In another way, therefore, two non-linear effects can occur: saturation and intermodulation. Any communication system evolves in a very constraining spectral environment. As mentioned previously, the presence of strong (interfering) signals close to the wanted channel can affect system performance. These signals can drive the system into a non-linear area and therefore create new unwanted frequencies which can overwhelm the wanted signal. So a system is linear if its response to a sum of excitation is equal to the sum of each excitation taken separately. Any system which does not satisfy this condition is said to be nonlinear. The frequency mixer and the LNA, which are the subject of this report, are devices whose analysis is likened to that of a nonlinear system.

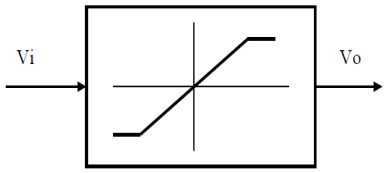


Figure 3.4 Non-linear system

Around the point V_i with low variation "$V_i \approx 0$", 1' the expression of the output V_o in the form of the Taylor series is written:

$$V_o = \alpha_0 + \alpha_1 V_i + \alpha_2 V_i^2 + \alpha_3 V_i^3 + \cdots \sum_{n=0}^{\infty} \alpha_n V_i^n \tag{3.2}$$

The coefficients α_n are assumed to be independent in frequency.

α_0 represents the DC offset voltage $\alpha_1 V_i$ is the first order term (liner), $\alpha_2 V_i^2$ is the second order term (quadratic term). If the system is linear the coefficients α_i are such that $\alpha_1 > \alpha_2 > \alpha_3 > \cdots$. For reasons of simplification of analysis, terms higher than third order are neglected.

Suppose the input signal V_i is sinusoidal $V_i = A cos\omega t$ the response relating to the nonlinear system will be [36]:

$$V_o = \alpha_1 A cos\omega t + \alpha_2 A^2 cos^2 \omega t + \alpha_3 A^3 cos^3 \omega t \tag{3.3}$$

In expression (3.3), note that we do not involve the DC component α_0, we assume that the reasoning is done in dynamic regime, in practice such a component corresponds to the polarization of nonlinear elements. After trigonometric expansion, Eqs, (3.3) becomes:

$$V_0 = \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4} cos\omega t + \frac{\alpha_2 A^2}{2} cos2\omega t + \frac{\alpha_3 A^3}{3} cos3\omega t \quad (3.4)$$

At the fundamental frequency the gain is equal to:

$$G_V = \alpha_1 A + \frac{3\alpha_3 A^3}{4} \quad (3.5)$$

In the case, where the amplitude A is small, the term $\frac{3\alpha_3 A^3}{4}$ can be neglected. Note also the growth of A^n proportionally with respect to the n^{th} harmonic.

Intermodulation also reflects the effect of non-linearity (harmonic distortion), it occurs when two signals, very closes in frequency, are present at the input of the system. Indeed when two signals of different frequencies are applied to a nonlinear system, at the output of this one are signals which are not harmonics of the original frequencies but a combination of these two frequencies, it is the intermodulation phenomenon, its effects are harmful

and can corrupt the useful signal. So at the output of the system, in addition to the harmonic distortion we get intermodulation.

Consider two sinusoidal signals applied to a nonlinear system:

$$V_i = A_1 cos\omega_1 t + A_2 cos\omega_2 t \tag{3.6}$$

Let's replace in the expression (3.3):

$$V_o = \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \alpha_2(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^2 + \alpha_3(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^3$$

Or:

$$V_o = \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \alpha_2({A_1}^2 cos^2\omega_1 t + 2A_1 A_2 cos\omega_1 t cos\omega_2 t + {A_2}^2 cos^2\omega_2 t) + \alpha_3({A_1}^3 cos^3\omega_1 t + 3{A_1}^2 A_2 cos^2\omega_1 t cos\omega_2 t + 3A_1{A_2}^2 cos\omega_1 t cos^2\omega_2 t + {A_2}^3 cos^3\omega_2 t)$$

Or again:

$$V_o = \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t)$$

$$+\frac{\alpha_2}{2}A_1^2 + \frac{\alpha_2}{2}A_1^2 cos2\omega_1 t + \frac{\alpha_2}{2}A_2^2 cos2\omega_2 t + \frac{\alpha_2}{2}A_2^2 + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)\, t$$

$$+ \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2)\, t$$

$$+\frac{3}{4}\alpha_3 A_1^3 cos\omega_1 t + \frac{\alpha_3 A_1^3}{4} cos3\omega_1 t + \frac{3}{4}\alpha_3 A_2^3 cos\omega_2 t + \frac{\alpha_3 A_2^3}{4} cos3\omega_2 t$$

$$+\frac{3}{2}\alpha_3 A_1^2 A_2 cos\omega_2 t + \frac{3}{2}\alpha_3 A_1^2 A_2 \cos(2\omega_2 - \omega_1)t$$

$$+\frac{3}{2}\alpha_3 A_1 A_2^2 cos(2\omega_2 + \omega_1)t + \frac{3}{2}\alpha_3 \frac{A_1 A_2^2}{2}\cos\omega_1 t$$

We can rewrite this expression by arranging the terms, so as to reveal the components that interest us. We will therefore have:

$V_o = \frac{\alpha_2}{2}(A_1^2 + A_2^2)$ Continuous term

$+\alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t)$ Amplified useful signal

$+\frac{\alpha_2}{2}(A_1^2 cos2\omega_1 t + A_2^2 cos2\omega_2 t)$ Harmonic 2 of ω_1 and ω_2

$+\frac{3}{4}\alpha_3(A_1^3 cos\omega_1 t + A_2^3 cos\omega_2 t)$

$+\frac{3}{2}\alpha_3(A_1^2 A_2 cos\omega_1 t + A_1 A_2^2 \cos 2\omega_2 t)$

$+\alpha_2 A_1 A_2(\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t$ 2nd order intermodulation

$+\frac{\alpha_3}{4}(A_1^3 cos3\omega_1 t + A_2^3 cos3\omega_2 t)$ Harmonic 3 of ω_1 and ω_2

$+\frac{3}{2}\alpha_3 A_1 A_2[A_1 cos(2\omega_1 + \omega_2)t + A_2 \cos(2\omega_2 + \omega_1)$ 3rd order intermodulation

$+\frac{3}{2}\alpha_3 A_1 A_2[A_1 cos(2\omega_1 - \omega_2)t + A_2 \cos(2\omega_2 - \omega_1)t]$ 3rd order intermodulation

The frequency response of this analysis presents multiple lines as shown in Figure 3.5. We see that around the useful frequencies ω_1 and ω_2 are superimposed two very close lines $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ called intermodulation lines of order 3, which cannot be eliminated by filtering. In general, the intermodulation lines of order *k (k integer)* are located at frequencies "$n\omega_1 \pm m\omega_2$" *(n, m integers)* with the sum *n* + *m* equal to *k*.

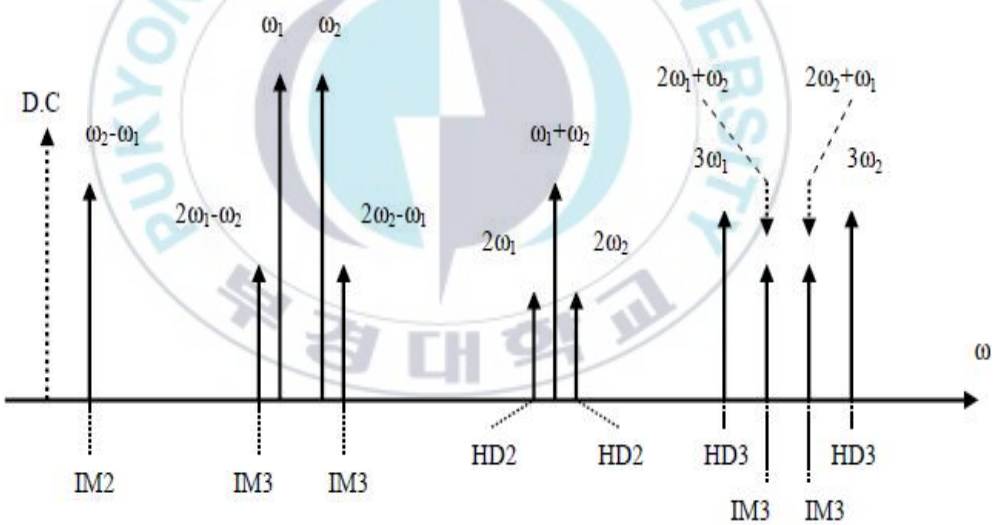


Figure 3.5 Spectrum at the output of nonlinear system

3.3 Important features of Mixers

The constant growth of requirements relating to the quality of RF functions make it more and more complex to validate these devices, and require knowledge of the definitions and terminologies necessary for the characterization of RF functionalities. To this end, we discuss the principles and definitions of the main figures of merit adopted to characterize RF devices and in particular mixers and LNAs [37-39].

As a result, the most useful analytical demonstrations and equations will be processed and will support and validate, in addition to simulations, the various performance concepts.

3.3.1 Level in dBm

While power is generally defined in watts *(W)* that in the field of radio frequencies is defined in *dBm* unit which is nothing other than the decibel *(dB)* relative to the mw, namely:

$$Power\ \ (dBm) = 10\log(\frac{Power(Watts)}{1mW}) \tag{3.7}$$

Also the input and output impedances of the devices (amplifiers, mixers) have in most cases a normalized value equal to 50Ω.

3.3.2 Conversion Gain (CG)

Each element of any RF transmitter/receiver system receives an input voltage V_{RF} with a power P_{RF} and generates an output signal V_{IF} with a power P_{RF} we can then define the gain of conversion into power by the relation:

$$\mathrm{CG} = 10\log\frac{available\ \ power\ \ at\ \ the\ \ output\ \ frequency}{available\ \ power\ \ at\ \ the\ \ input\ \ frequency} \quad (3.8)$$

$$G_{V,dB} = 20\log(\frac{V_{IF}}{V_{RF}}) \qquad G_{VP,dB} = 10\log(\frac{P_{IF}}{P_{RF}}) =$$

$$10\log(\frac{\frac{V_{IF}^2}{R_{IF}}}{\frac{V_{RF}^2}{R_{RF}}}) \quad (3.9)$$

The conversion gain is a critical parameter whose effects can degrade the noise figure and the linearity of the system. Effectively when determining the total system noise figure, the noise of the stage subsequent to any element in the chain can be amplified or attenuated by the gain.

3.3.3 Noise Figure (NF)

This is a factor that allows us to assess the quality of a device based on the noise it generates. In fact, it allows us to quantify the noise level in a

signal; this factor becomes more and more important when dealing with low input powers.

We define the noise figure of a device as being the ratio of the noise power available at the output of the device compared to the part of this power due to the internal impedance of the source placed at the input and assumed to be carried at a temperature of 290° *K*. In other words, the noise factor is the degradation, due to the component, of the signal to noise ratio "SNR" of the source, assumed to be raised to 290° *K*. This is, therefore, the ratio between the SNR at the input of the device and the SNR at the output of the device Eqs. (3.10). [40].

$$NF = \frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{Nout}} = \frac{SNR_{in}}{SNR_{out}} \tag{3.10}$$

where $(SNR)_{in}$ and $(SNR)_{out}$ are respectively the signal to noise ratio measured at the input and the output of the device. S_{in} and N_{in} are the input noise signal and power while S_{out} and N_{out} represent the output noise signal and power.

Thus, any system can be represented by equivalent noise sources

reported at the input of a noise-free quadrupole, a voltage source $\overline{V_n^2}$ and a current source $\overline{I_n^2}$ as illustrated in Figure 3.6 [41].

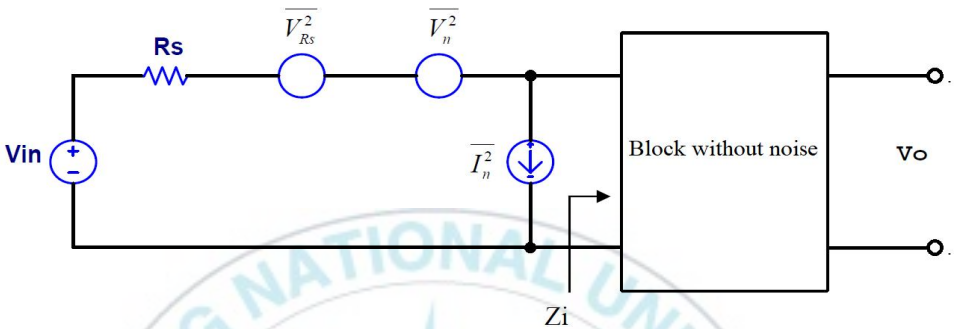


Figure 3.6 Representation of noise in a nonlinear system

R_s is assumed to be the only source of noise at the input of the system (it can represent the radiation resistance of an antenna), then the noise generated before it passes through the system is Eqs.(3.11), (3.12).

$$\overline{V_n^2} = 4kTRs \tag{3.11}$$

where $k=1.38x10^{-23}$ *J/K* (*Boltzmann constant*) and T represents the temperature in Kelvin. For the system shown, the noise figure (*NF*) is expressed by Eqs. (3.12).

$$NF = 1 + \frac{\overline{(V_n + I_n R_S)^2}}{4kTR_S} \tag{3.12}$$

Therefore, the noise restricts the use of signals and influences the performance of the entire system.

However, a system cannot completely eliminate noise affecting signals and in this case, the minimum achievable *NF* is 0*dB*.

In reality the architecture of a transmitter/receiver is made up of a set of cascaded stages, as shown in Figure 3.7 the overall noise figure then takes into account the different levels of impedances and possibly the gains of each stage [42].

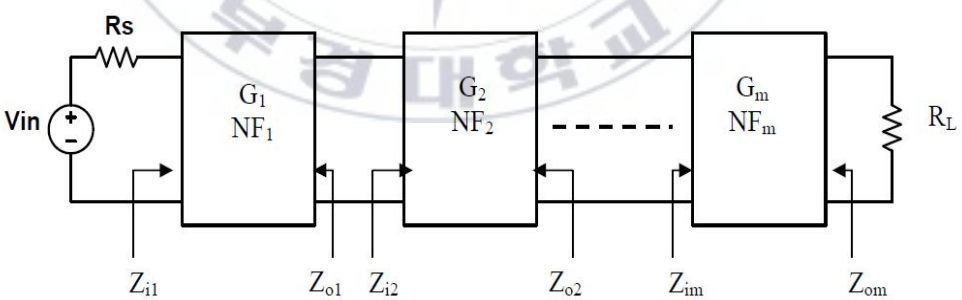


Figure 3.7 Cascading non-linear stages

Taking into account the equivalent sources of noise and associating two stages, the overall *NF* is obtained by the relationship:

$$NF_2 = \frac{4kTR_S + \overline{(V_{n1} + I_{n1}R_S)^2}}{4kTR_S} + \frac{\overline{(V_{n2} + I_{n2}R_S)^2}}{G_V^2(4kTR_S)} \frac{(\frac{R_{i2}}{R_{o2} + R_{i2}})^2}{(\frac{R_{i1}}{R_S + R_{i1}})^2} \quad (3.13)$$

In the case of a reception chain of several cascaded floors, the overall noise figure can be deduced from the FRIIS equation (3.8):

$$NF_{total} = NF_{1,Z_S} + \frac{NF_{2,Z_{01}} - 1}{G_1} + \cdots + \frac{NF_{m,Z_{(m-1)}} - 1}{G_1 \ldots G_{(m-1)}} \quad (3.14)$$

Along with;

$$G_m = \left(\frac{Z_{i,m}}{Z_{o,(m-1)} + Z_{i,m}}\right)^2 G_{V,m}^2 \frac{Z_{o,(m-1)}}{Z_{o,m}} \quad (3.15)$$

where $NF_{m,Z_{(m-1)}}$ is the noise figure (*NF*) of the m^{th} stage, characterized as a function of a noise resistance equal to the output impedance of the previous stage *(m-1)*.

$Z_{i,m}$ is the input impedance of the m^{th} stage.

$Z_{o,m}$ is the output impedance of the m^{th} stage.

$G_{V,m}$ is the gain of the m^{th} stage.

From equation (3.14), the contribution of each stage to the overall NF decreases as the gain of the stage preceding it increases. Thus, we notice that the noise of the first stage of a cascade chain is preponderant; this is the case of the noise of the LNA in a receiver unit that we will deal with in chapter 4.

Also, this same formula (3.14) highlights the importance of the gain noise factor (G_1) of the first LNA stage. On its own, it conditions the noise figure and also the interception point of order 3, which we can see in the previously paragraph, of the whole system.

3.3.4 Isolation

Isolation measures the level of power leakage coupled from one port to another of the various elements of an RF chain. In this present work, we are interested in the isolations between the mixer and LNA ports, the specifics of which are usually in the mixer, in this case, LO to IF isolation and LO to RF isolation.

As mentioned in Figure 3.8, these leaks degrade the received signal, nevertheless the LO/IF isolation can easily be attenuated by a low pass filter, this during the LO frequency appearing on the IF port is very far from that of IF. This is not the case when the LO frequency leaks on the RF port because these two frequencies are close. This leak is of more concern

because it allows re-transmission through the antenna of the LO frequency if the mixer is used in the first mixing stage in a wireless receiver.

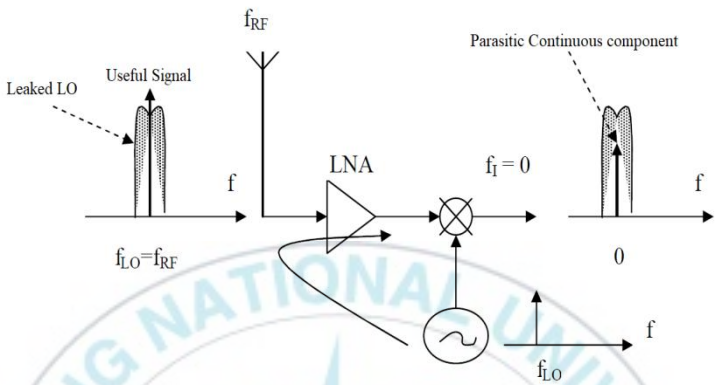


Figure 3.8 Leakage of LO in RF chain

In a mixer, it is possible to improve isolation by using differential structures whereby unwanted signal cancellation is possible. Indeed the property used is that two signals of the same amplitude cancel each other out when they are added in phase opposition.

3.4 Topology of Active Transistor Mixers

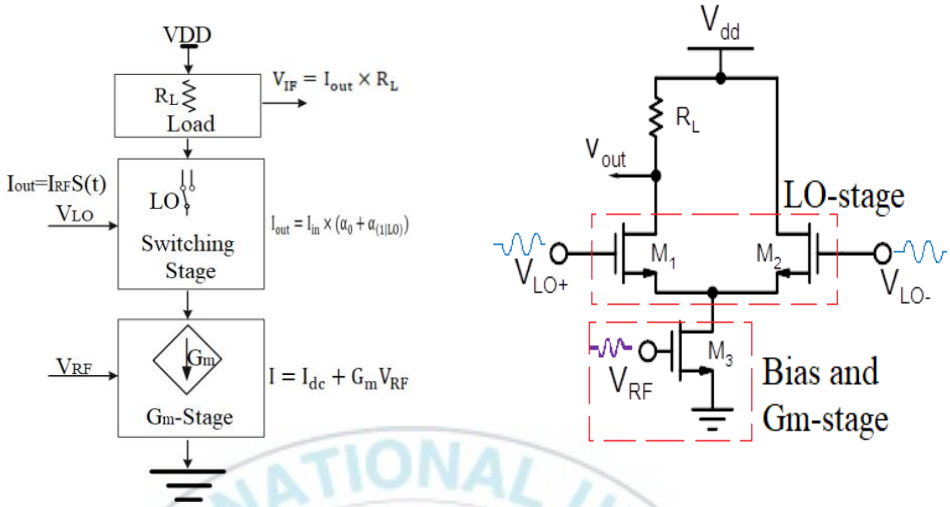
Unlike passive topologies, active mixers have the advantage of having a large conversion gain without requiring a high LO switching level. This feature is useful for combining frequency change and amplification together. These mixers can be made either with bipolar (BJT) or field effect (FET) transistors and their mixing principles result from the nonlinear variation of

transconductance under the control of the LO signal. Moreover, the choice of high-frequency CMOS has advantages. It generates less noise and has low levels of distortion. In addition, MOS is insensitive to fluctuations in input voltages that bipolar in addition to their low power consumption.

Three types of mixers are classified as unbalanced, single-balanced, and double-balanced, in accordance with the mixing process of RF and LO signal. Each of these architectures will be discussed and analyzed in the following.

3.4.1 Unbalanced Mixer

Figure 3.9 shows the schematics of the unbalanced mixer along with the G_m-stage and the switching point. It is obvious from Figure 3.9 (a) that this structure is named unbalanced mixer, because there is only one output. G_m-stage's purpose is to cover up the voltage signal to current one by simply configuring common source. The switching stage, as mentioned previously, translates signals from radio frequency to intermediate frequency over a period of time by switching.



a) b)

Figure 3.9 Specific concept of unbalanced mixing (a) and Unbalanced mixer (b)

To consider the conversion gain shown in Figure 9 (b) for the unbalanced current-commutating mixer, let's consider Figure 3.9 (a) for its condensed form.

V_{IF} and CG may be written as follows:

$$V_{out} = I_{out}R_L = I_{RF}\ S(t)R_L = R_L(I_{DC} + G_m V_{RF})(S_0 + S_1\cos(\omega_{LO}t) + S_2\cos(2\omega_{LO}t) + \cdots) = R_L(I_{DC} + G_m V_{RF})(\frac{1}{2} + \frac{2}{\pi}\cos(\omega_{LO}t) + \frac{2}{3\pi}\cos(3\omega_{LO}t)) \quad (3.16)$$

$$\mathrm{CG} = \frac{|V_{IF}|}{|V_{RF}|} = \frac{G_m R_L}{\pi} \tag{3.17}$$

where the output voltage is V_{out}, the output current is I_{out}, the load resistor is R_L, and switching wave is S(t). I_{DC} is the current source of DC current, the input voltage is V_{RF} of Gm-stage.

3.4.2 Single Balanced Mixer

Low isolation and conversion gain are the main issues are in unbalanced mixers. A Single-balanced mixer is introduced as shown in Figure 3.10 to solve these issues and improve the efficiency of the mixers. The switching stage and the output are differential as shown by these sorts of mixers. The whole differential architectural process in the cancelation of the switching stages DC component and thus improves isolation from the RF-IF. The output is differential the conversion gain usually doubles that the single-ended output gain. However, the output offset is much less than the previous one in a single-balanced mixer.

The conversion gain of single balanced mixer is given below:

$$V_{out} = I_{RF}(S\left(t - \frac{T_{LO}}{2}\right) - S(t))R_L = I_{RF}\ S(t)R_L$$

$$V_{out} = R_L(I_{DC} + G_m V_{RF})(2S_1\cos(\omega_{LO}t) + 2S_2\cos(3\omega_{LO}t) + \cdots)$$

$$= R_L(I_{DC} + G_m V_{RF})(\frac{4}{\pi}\cos(\omega_{LO}t) + \frac{8}{3\pi}\cos(3\omega_{LO}t)) \quad (3.18)$$

$$\mathrm{CG} = \frac{|V_{IF}|}{|V_{RF}|} = \frac{2G_m R_L}{\pi} \quad (3.19)$$

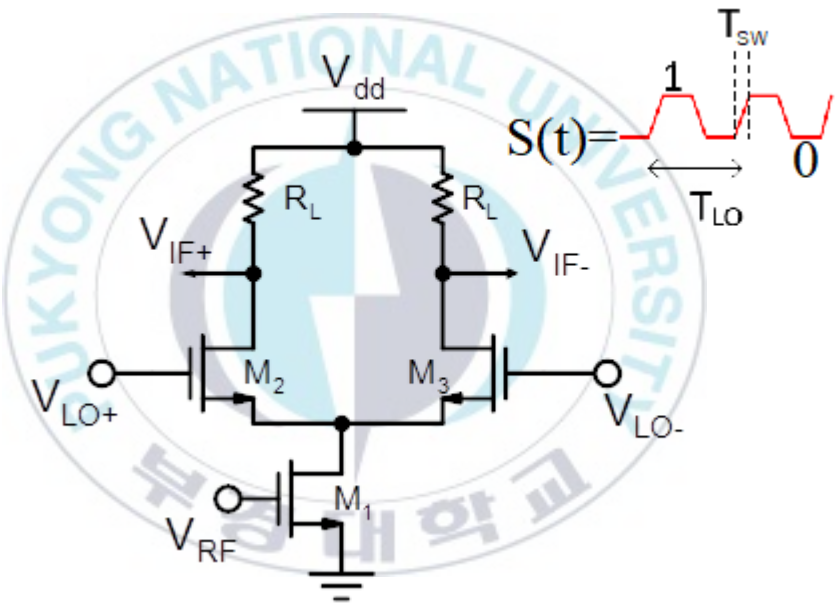


Figure 3.10 Single-Balanced Mixer

By analyzing the impact of input matching and assuming the switches are not optimal (rising and falling times *(T_{sw})* are not zero), the conversion gain is as given Eqs. (3.20):

$$\mathrm{CG} = \left(\frac{Z_m}{Z_{RS} + Z_m} \cdot \alpha_m\right).\left(\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\right).\left(\frac{g_{m2}}{\sqrt{g_{m2}^2 + \omega^2 C_T^2}}\right)\left(\frac{2R_{L-max}g_{m3}}{\pi}\right) \quad (3.20)$$

Where α_m defines an output waveform to the current source from the corresponding input network (Gm-stage). T_{sw} and T_{LO}, respectively, are the switching times and the LO signals.

The switching period time is dependent on the DC current bias and LO power as well as the size of the transistors in the switching point.

$$T_{sw} = T_{sw}(P_{LO}, I_{DC}, SW\ \ size) \tag{3.21}$$

The isolation from the port can be described as:

$$V_{out} = R_L(I_{DC} + G_m V_{RF})(\frac{4}{\pi}\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\cos(\omega_{LO}\mathrm{t}) + \cdots)$$

$$V_{LO-IF} = \frac{4}{\pi}R_L I_{DC}\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\cos(\omega_{LO}\mathrm{t})$$

$$V_{RF-IF} = 0 \tag{3.22}$$

Since it is confirmed, the input port is completely integrated from the output port in a single balanced mixer which is an advantage for this design compared to the previous one which suffers from the issue of port feedthrough.

3.4.3 Double- Balanced Mixer

As shown in Figure 3.11 double-balanced mixer is proposed to improve conversion gain and isolation problems of single-balanced mixer. Through easy sentences, in kind of a fully differential architecture, the double-balanced mixers are consisting of two single-balanced mixers. Conversion gain from double-balanced mixers has double gain relative to previous ones, and the output port LO leakage will be canceled out. However, such improvements gain at the cost of additional power consumption [43]. As pointed out earlier, the dual-balance mixer consisted of two single-balanced mixers, and the simple result is that the dual-balanced mixer's power output is twice as much as a single-balanced mixer.

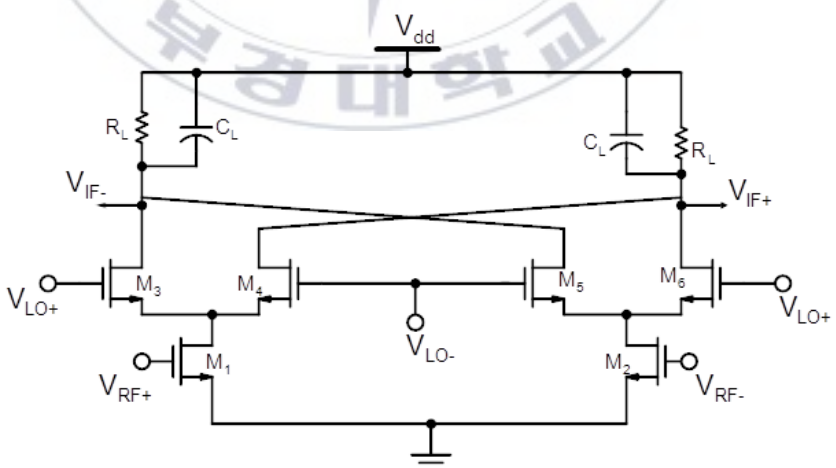


Figure 3.11 Double-Balanced Mixer

The major components of the double-balanced mixer are illustrated in the following by Eqs. (3.23).

$$\mathrm{CG} = \frac{|V_{IF}|}{|V_{RF}|} = \frac{4G_m R_L}{\pi} \tag{3.23}$$

By analyzing the impact of input matching and assuming the switches are not optimal (rising and falling times *(T_{sw})* are not zero), the conversion gain is as given Eq. (3.18):

$$\mathrm{CG} = \left(\frac{Z_m}{Z_{RS}+Z_m}\cdot\alpha_m\right).\left(\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\right).\left(\frac{g_{m2}}{\sqrt{g_{m2}^2+\omega^2 C_T^2}}\right)\left(\frac{4R_{L-max}g_{m3}}{\pi}\right) \tag{3.24}$$

The isolation from the port can be described as:

$$V_{out} = 2R_L(I_{DC}+G_m V_{RF})\left(\frac{4}{\pi}\mathrm{Sinc}\left(\frac{T_{sw}}{T_{LO}}\right)\cos(\omega_{LO}\mathrm{t})+\cdots\right)$$

$$V_{LO-IF} = 0$$

$$V_{RF-IF} = 0 \tag{3.25}$$

It becomes obvious that, according to its special configuration, the double-balanced mixer greatly improves the isolation between various ports.

3.5 Circuit Design and Analysis

The designed to 24GHz and 77GHz and detect obstacles around the vehicle, to help park a vehicle in a parking lot, to brake automatically, control the pace of the vehicle intelligently. The best known application is ACC, which assists the driver and increases comfort by adapting vehicle speed to the flow of traffic. Short-Range Radar corresponds to the anti-collision radar is intended to improve the safety of drivers and to anticipate driving in case of danger [45]. The future generation of vehicles will be able to communicate with each other about their relative positions, to alert each other about the traffic situation or the weather [46]. In the future all applications will be developed in the frequency band 77GHz-81GHz, allocated for this purpose, while the use of the band 24GHz is doomed to disappear [47], [48], [49].

In this work, we present low power, lowest noise figure and high-gain 24GHz RF down-conversion mixers including the Gilbert Cell for the short-range automotive radar. The circuit is fabricated using 65nm mixed signal RF CMOS process, and it is powered by 1.5V supply. The proposed circuit is designed utilizing a double-balanced topology using bias-offset technique to reduce power consumption and to get high conversion gain.

3.5.1 Structure of 24GHz Radar

The short range radar (SRR) works in pulse mode with covered distance of about 30 meters and it uses wide bandwidth. Radar for vehicle applications usually uses two frequencies 77GHz and 24GHz, to increase the safety of future car and avoid unnecessary collision. Also, 24GHz radar is easier to handle and it is the most used frequency but 77GHz is also consider. The SRR could cover a lot of applications such a parking aid, ACC with stop and go, pre-crash or collision warning, back-up function. It has also better performance in azimuth angle and in range measurements, thus suitable for automotive applications like parking aid, pre-crash detection, side object detection and blind spot detection. As describes in Figure 1.2 [47].

3.5.2 Design of 24GHz CMOS Mixer

The proposed CMOS down-conversion mixer is implemented using the 65μm RF CMOS process. This technology has been retained because of its good low noise performance and cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) have 120/140GHz, respectively. The mixer converts the input radio frequency (*RF*) 24GHz to an intermediate frequency (*IF*) 2.4GHz. The influence of the mixing stage of down-conversion mixer

as shown in Figure 3.12 on linearity has been previously investigated in literature. It depends on a great extent on the frequency of operation. At a high frequency where the parasitic capacitance associated with the transistors are very important. The low voltage ability of the trans-conductor is accomplished through offsetting the gate bias voltage of M_7&M_8 (M_9&M_{10}) to ensure simultaneously high input voltage domain for M_7&M_8 (M_9&M_{10}) at the supply of 1.5V. The design implements synchronous performance of M_7, M_8, M_9, & M_{10} at the saturation region by a comparatively large domain of the input signal levels. Parallel resistances (R_4=R_5) across a capacitor (C_4=C_5) will force some current and offers a feed forward possibility for the input signal, enhances the high frequency implementation of the floating voltage source.

$$G_m = \frac{I_{D7}-I_{D8}}{V_{RFin+}} = \frac{I_{D7}}{V_{RFin+}} - \frac{I_{D8}}{V_{RFin+}} \tag{3.26}$$

As we assumed that $V_{SG7} = V_{DD} - V_{RFin+}$ and $V_{SG8} = V_{RFin+} + V_{offseting}$.

The trans-resistance stage converts the down-converted current at IF back to voltage. It may be implemented using resistors or active loads, or a combination of the two to provide adjustability to the load resistance and achieve offset or device mismatch cancellation.

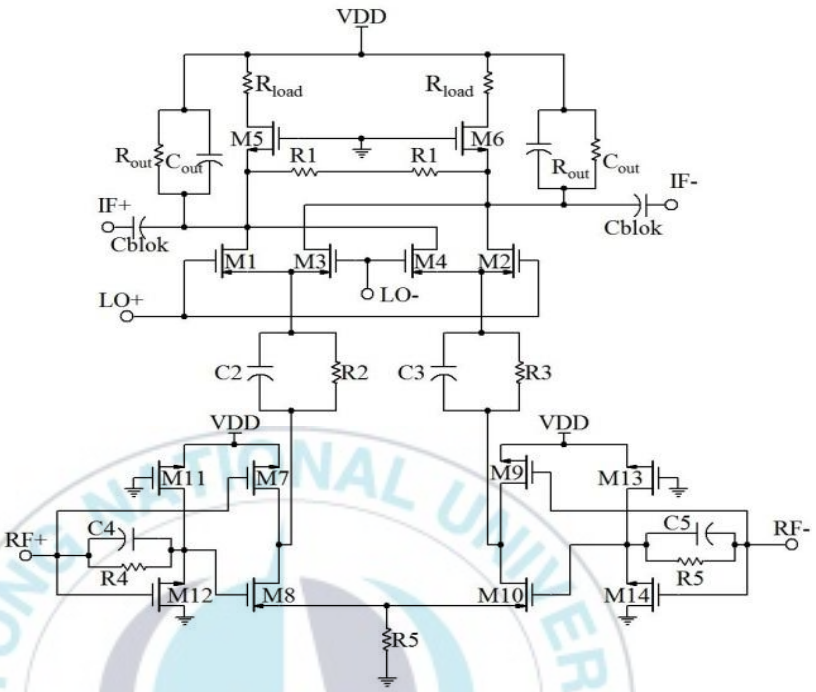


Figure 3.12 Proposed 24GHz CMOS down-conversion mixer

By introducing parallel resistor-capacitor (PRC) $R_4//C_4$, the RF signal occurring at the gates of M_7&M_8 (M_9&M_{10}) will be same as needed for the proper implementation of the circuit diagram. This configuration bias offset method is applicable at any RF frequency as long as the transistor is capable of providing a reasonable transconductance. So further enhance the linearity of the transconductance, threshold value modulation is ignored. Figure 3.12 illustrates the simulated is understandable that conversion gain of the double balanced mixer depends on the g_m of output load stage resistor R_{load} and RF stage transistors, the *W/L* ratio should be large for higher gain.

However, it should not be too large because larger transistors have higher gate-source parasitic capacitance which tends to limit the high frequency operation and increases the noise figure. The half circuit and consisting of M_7, M_8, M_{11}, & M_{12} these various values of offset voltage of V=435mV, for $(W/L)_7$=20μm/0.13μm and $(W/L)_8$=15μm/0.13μm. As described, the RF transconductor is combined to LO (local oscillator) stage prepared by cross-coupled differential inputs which is ended up in a low pass load to eliminate any unwanted high frequency composition in the IF (intermediate frequency) signal. The cross coupled LO stage is biased by RC in parallel combinations set at 21.6GHz instead of the conventional current sources to set-up a low-voltage operation and optimize the performance of the LO stage at 21.6GHz. Active loads are avoided at the IF of the mixer to decrease the noise figure at the baseband frequencies.

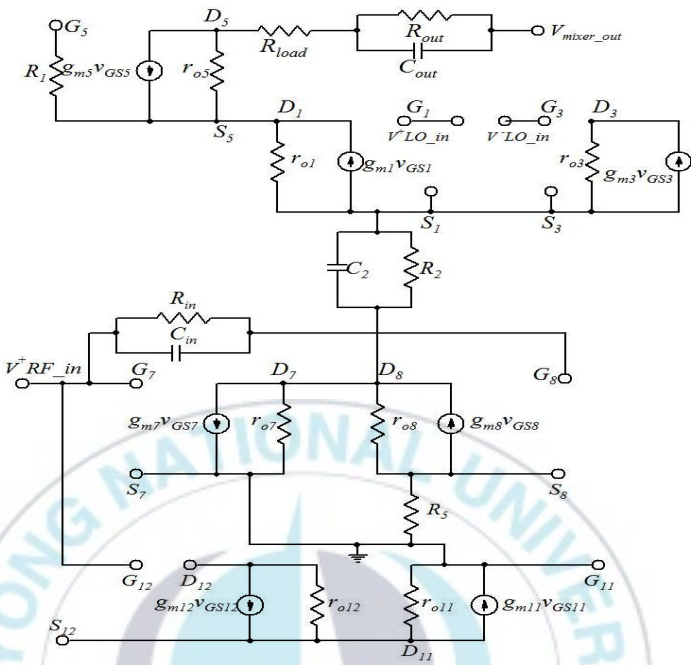


Figure 3.13 High-frequency small-signal model for the mixer

Figure 3.13 shows simplified high-frequency small-signal model for positive input side of the mixer. The simultaneous matching including the effect of the load impedance is considered for the simplified small-signal MOS models and M_5&M_6 are same type of value at the saturation region as $\mathrm{I_{ds5}} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_5(V_{gs5} - V_{thn})^2$; now, since M_5 is having the same parameters of M_6 $V_g=0$; $V_{d5}=V_{DD}$; $V_{sM5}=V_{sM1}$; $\mathrm{I_{dM_5}} = \mathrm{I_{dM_6}}$; $\mathrm{I_{dM_6}}=\mathrm{I_{dM_2}} + \mathrm{I_{dM_3}}$; now $\mathrm{V_{sM_1}} - \mathrm{R_2 I_L} = \mathrm{V_{dM_8}}$; $\mathrm{I_L} = \mathrm{I_{dM_1}} + \mathrm{I_{dM_4}} = \mathrm{I_{dM_5}}$. As shown in Figure 3.12 $\mathrm{I_{dM_{11}}} = \mathrm{I_{sM_{12}}}$ because R_4 is floating resistance and C_4 is open

circuited and $I_{gM_8}=0$ gate terminal. For M_1 PMOS verification from the simulation date PMOS to be in saturation $V_{gd}>V_{th}$ ($V_{gd}<V_{th}$, for NMOS to be in saturation) also ($V_{gs}<V_{th}$).

The proposed mixer core of mixing stages transistors M_1, M_3, M_4, & M_2 work in the saturation region, the current flow through it is $I_{dM1} = -\frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_1(-V_{s1} - V_{thp})^2$; V_{thp} and V_{thn} are threshold voltage of M_1 and M_5, μ_p and μ_n are mobility of charge carriers of PMOS and NMOS transistors respectively. W, L, and C_{ox} represent the transistor's width, length, and gate capacitance per unit area.

By applying the KCL at source node we get

$$C_{gs} = C_{gd} = \frac{C_{ox}WL}{2} = C_{gc}(V_s = V_d); \tag{3.27}$$

$Z_X=C_{in}//R_{in}$, $Z_Y=C_2//R_2$

For transistor M_7 as $V_{gs7}=V_{g7}-V_{s7}$, $V_{b7}=0$ by inserting these values and rearranging, we will get V_{s7} Equation (3.33).

$(V_{o7}- V_{b7})C_{db7}= V_{b7} C_{db7}$; $V_{g7}=V_{i7}$.

$$(V_{o7} - V_{i7})C_{gd7} + \frac{V_{o7}-V_{s7}}{r_{o7}} + g_{m7}V_{gs7} = 0$$

$$(V_{o7} - V_{i7})C_{gd7} + \frac{V_{o7}-V_{s7}}{r_{o7}} + (V_{i7} - V_{s7}) = 0 \tag{3.28}$$

$$(V_{i7} + V_{s7})C_{gd7} - V_{s7}C_{cb7} + g_{m7}V_{gs7} + \frac{V_{o7} - V_{s7}}{r_{o7}} = 0 \tag{3.29}$$

$$(V_{i7} - V_{s7})C_{gs7} + (V_{i7} - V_{o7})C_{gd7} = I_{in} \tag{3.30}$$

$$(V_{o7} - V_{i7})C_{gd7} + V_{o7}C_{gd7} + \frac{V_{o7} - V_{s7}}{r_{o7}} + g_{m7}V_{gs7} = 0 \tag{3.31}$$

$$V_{o7}\left(C_{gd7} + C_{gd7} + \frac{1}{r_{o7}}\right) - V_{i7}\left(C_{gd7} - g_{m7}\right) - V_{s7}(1 + \frac{1}{r_{o7}}) = 0 \tag{3.32}$$

By rearranging Equation (3.28), we get the value of voltage V_s at source node.

$$V_{s7} = \frac{V_{i7}\left(g_{m7} + C_{gs7}\right) + \frac{V_{o7}}{r_{o7}}}{C_{gs7} + C_{bs7} + g_{m7} + \frac{1}{r_{o7}}} \tag{3.33}$$

As we assumed V_g=V_i for NMOS transistor, M_7 and then voltage gain of M_7 is $A_v = \frac{V_o}{Vi} = \frac{V_o}{Vg}$. By rearranging Equation (3.31) and (3.32), we get Equation (3.33), by inserting these Equations (3.32) and (3.33), we will get A_v Equation (3.37).

$$V_{o7}\left(C_{gd7} + C_{gd7} + \frac{1}{r_{o7}}\right) - V_{i7}(C_{gd7} - g_{m7}) - \frac{V_{i7}(g_{m7} + C_{gs7}) + \frac{V_{o7}}{r_{o7}}}{C_{gs7} + C_{bs7} + g_{m7} + \frac{1}{r_{o7}}}(1 + \frac{1}{r_{o7}}) = 0 \tag{3.34}$$

$$V_{o7}\left(C_{gd7} + C_{gd7} + \frac{1}{r_{o7}}\right)\left(C_{gs7} + C_{bs7} + g_{m7} + \frac{1}{r_{o7}}\right)V_{i7}\ \left(C_{gd7} - g_{m7}\right)\left(C_{gs7} + C_{bs7} + g_{m7} + \frac{1}{r_{o7}}\right) - \left(V_{i7}\left(g_{m7} + C_{gs7}\right) + \frac{V_{o7}}{r_{o7}}\right)\left(1 + \frac{1}{r_{o7}}\right) = 0 \tag{3.35}$$

$$V_{o7}\left(\frac{(C_{gd7}+C_{gd7}+\frac{1}{r_{o7}})(C_{gs7}+C_{bs7}+g_{m7}+\frac{1}{r_{o7}})}{(1+\frac{1}{r_{o7}})}+\frac{1}{r_{o7}}\right)$$

$$-V_{i7}\left(\frac{(C_{gd7}-g_{m7})\left(C_{gs7}+C_{bs7}+g_{m7}+\frac{1}{r_{o7}}\right)}{(1+\frac{1}{r_{o7}})}+\left(g_{m7}+C_{gs7}\right)\right)=0 \tag{3.36}$$

$$A_v=\frac{V_o}{Vi}=\frac{r_{o7}(C_{gd7}-g_{m7})\left(C_{gs7}+C_{bs7}+g_{m7}+\frac{1}{r_{o7}}\right)+(g_{m7}+C_{gs7})(1+\frac{1}{r_{o7}})}{r_{o7}\left(C_{gd7}+C_{db7}+\frac{1}{r_{o7}}\right)\left(C_{gs7}+C_{bs7}+g_{m7}+\frac{1}{r_{o7}}\right)+\left(1+\frac{1}{r_{o7}}\right)} \tag{3.37}$$

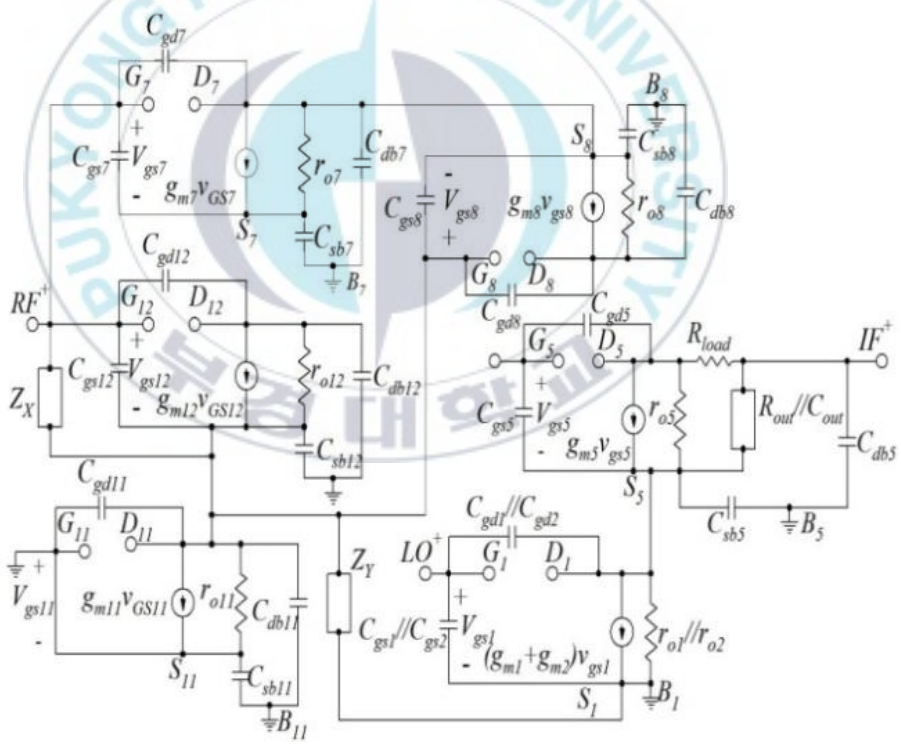


Figure 3.14 Small signal half-circuit model of the proposed mixer

3.6 Results and Discussions

3.6.1 Transient and Harmonics responses

The whole schematic of the proposed mixer is illustrated in Figure 3.12 using Cadence software in 65nm RF CMOS process. The mixer manned with 1.5V supply voltage. The proposed mixer has been utilized two port measurements. Again using ADS analysis, the RF power is swept 10dBm and LO power is swept from -10dBm to 5dBm for the simulation, Figure 3.15 and 3.16 gives the frequency spectrum of V_{RF} and V_{IF}. The presence of a harmonic balance at RF and LO frequencies are respectively 24GHz and 21.6GHz which provides an IF frequency of 2.4GHz for down-conversion receiver. The input and output voltage amplitudes in a transient analysis are depicted in Figure 3.15 and 3.16. Based on the data from the peak-markers, we can estimate the voltage gain of this mixer as: $G_V = 20\log(\frac{V_{IF}}{V_{RF}})$

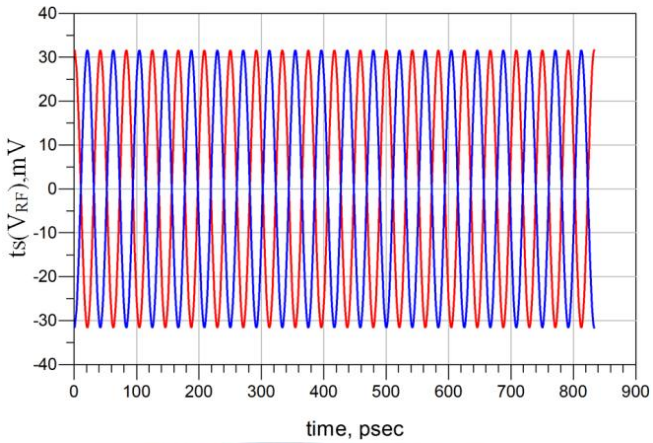


Figure 3.15 Input signal

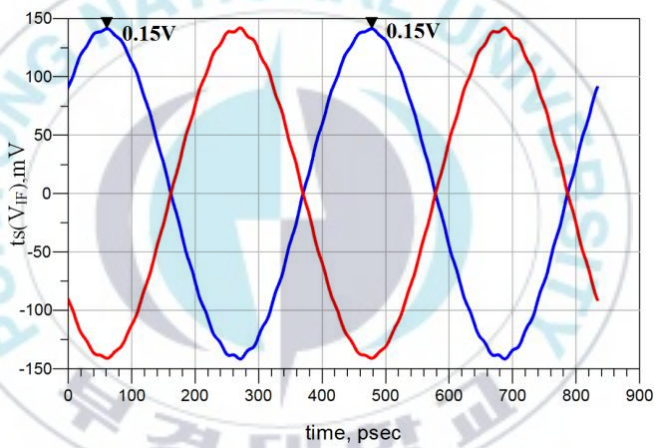


Figure 3.16 Output signal

The following Figure 3.17 shows that the output a frequency of RF-LO value equal to 2.4GHz, however a 24GHz line of others unwanted harmonics are due to the non-linearity of the circuit. That can be eliminated by the use of filter to “only restore” the desired frequency. The proposed circuit showed the highest conversion gain of 14.8dB as compared to recently reported research results [61], [62], [63], [64].

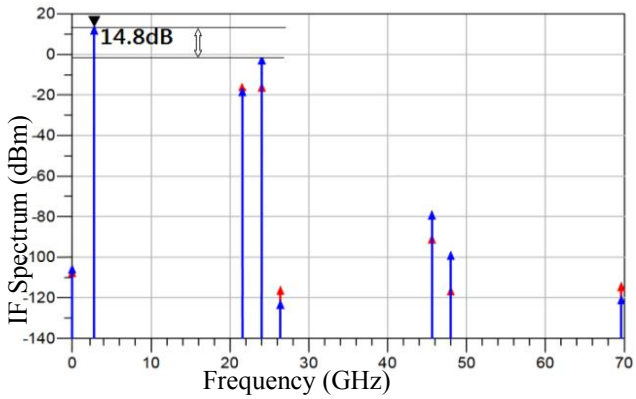


Figure 3.17 Conversion gain of proposed mixer

3.6.2 Noise Figure

It can be seen from that curve noise in the input and in the output, are shown in Figure 3.18 and 3.19.

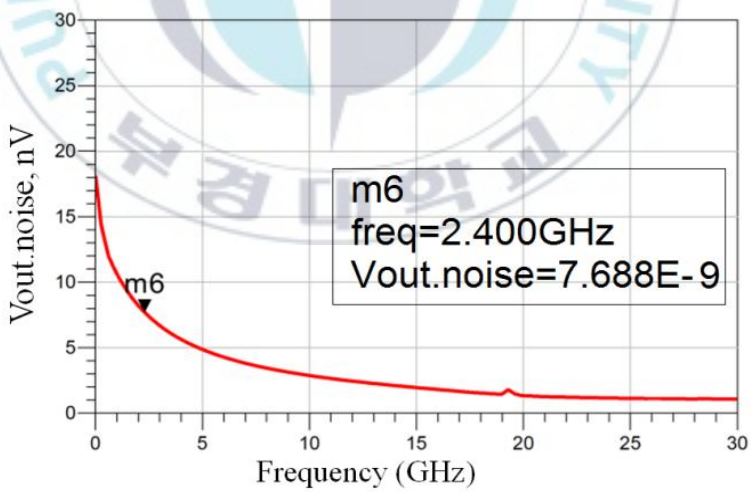


Figure 3.18 Output noise

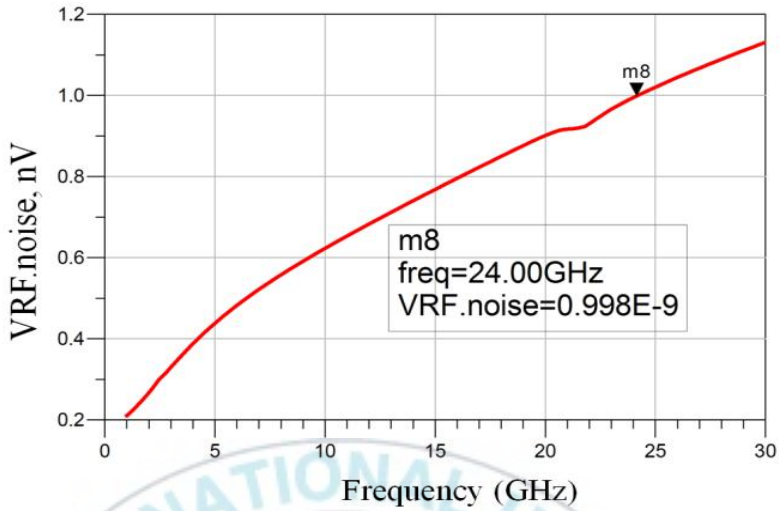


Figure 3.19 Input noise

By comparing Figure 3.18 and 3.19 the relationship between Input Noise, Output Noise and the Conversion Gain, $NF = \frac{N_{out}}{N_{in} \cdot CG}$ we get the value of voltage the Noise Figure of 2.87dB.

3.6.3 Order 3 interception point (IIP3)

As shown in Figure 3.20 the 1dB compression point (P1dB) of mixer is measured approximately -1.2dBm. The proposed mixer achieves the third order intercept as high as 3.2dBm and the power consumption of 1.57mW with supply voltage of 1.5V.

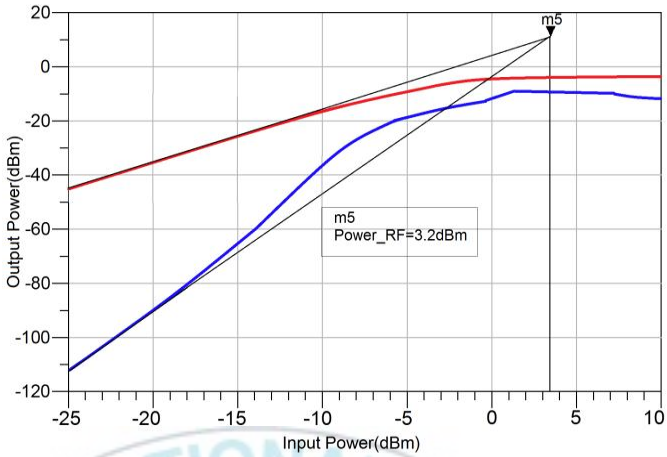


Figure 3.20 Third order interception point (IIP3)

The whole schematic of the proposed mixer is already illustrated in Figure 3.12 it consists of n/pMOS transistors the simulated is understandable that conversion gain of the double balanced mixer depends on the g_m of output load stage resistor R_{load} and RF stage transistors, the *W/L* ratio should be large for higher gain. The layout of the proposed down-conversion mixer is shown in Figure 3.21. The circuit is implemented in 65nm RF CMOS process. The chip occupies $0.41\times0.41mm^2$ including pads, and $0.108\times0.109mm^2$ without pads. The RC capacitors 1.5pF combinations employed System On-Chip at supply voltage. All resistors and capacitors are implemented using P+Poly Salicide-Resistor (*ppcres*) and 2-Node-Metal-Insulator-Metal-Capacitor.

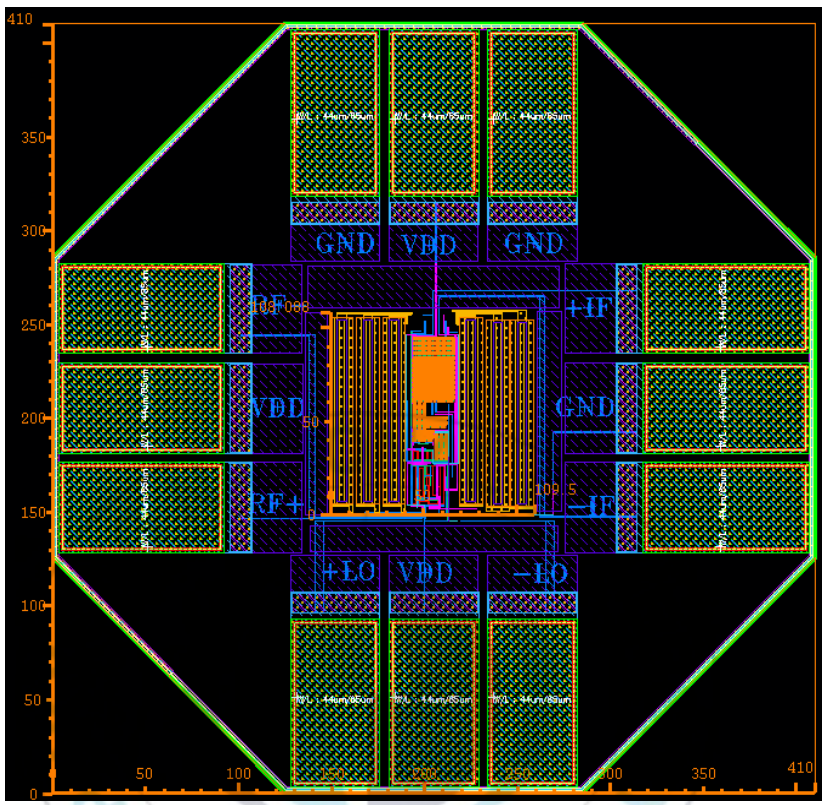


Figure 3.21 The proposed mixer layout

To verify that in Figure 3.12 is operating as expected, simulations are carried out using ADS software, calculation is extracted using high-frequency small signal equivalent model using Figure 3.13. As shown in Figure 3.17, the highest conversion gain of 14.8dB can be realized and noise figure is 2.87dB of the proposed mixer at 24GHz. The performances of this present CMOS mixer are compared in Table 2. We note that the design we have proposed shows good performance in terms of conversion gain, power

consumption of 1.54mW, also the IIP3 point levels and the1dB compression point remain admissible.

Table 3.1: Shows the comparison of this work and some of the 24GHz CMOS mixers, reported in the recent literature.

Performance	**This work**	[61]	[62]	[63]	[64]
Frequency (GHz)	**24**	24	24	24	24
Conversion Gain (dB)	**14.8**	23.36	11.3	2	8.376
Noise Figure (dB)	**2.87**	5.32	14.2	28	11.6
Input P1dB (dBm)	**-1.2**	-27	-13.5	8	-8.4
IIP3 (dBm)	**3.2**	-17.4	-1	20	-
Technology (nm)	**65**	180	130	180	180
Power Consumption (mW)	**1.54**	31.65	27.8	53	5.65
Chip area mm^2	**0.10×0.10**	0.8×0.6	0.4×0.5	0.6×0.8	1.06×0.9

3.7 Summary

In this chapter, we have calculated the most important parameters characterizing the double balanced Gilbert Cell mixer and we are interested in improving its linearity by the method bias offset to have a high-linear mixer with 65nm CMOS technology for applications is proposed at 24 GHz. The mixer is measured using the ADS in 1.5 supply voltage. The proposed circuit showed as a result, active topologies have the advantage of offering a good conversion gain of 14.8dB. The designed sensor has low cost and low power since it is realized using CMOS process. The proposed sensor showed the lowest noise figure of 2.87dB and the smallest chip occupies $0.41\times0.41mm^2$ including pads, and $0.108\times0.109mm^2$ without pads as compared to recently reposted research results.

Besides, the power consumption is reduced compared to other works.

Chapter 4

4. Design of Low Power and High Linearity CMOS RF Front-End Receiver in 65nm Technology for 24GHz Application

4.1 Background

The rapid growth of radio frequency and wireless communications has seen resurgence especially in the last decade. Low-voltage, low power, and merged circuits are the most noticeable subjects for merged circuits design. Some standards for wireless communication have been introduced for short-range radar (SRR) and long-range radar (LRR) communications. Since the wireless communication system is very lossy, the received signal from the antenna has a very weak force. Hence, low noise amplifier (LNA) has to be used after the antenna to amplify the signal at the receiver. Moreover, in order to translate the amplified signal to the wanted lower frequency to allow channel selection filtering, using another device in receiver topology is very important, which is a mixer. In point of fact, the mixer multiplies the signal to another signal that generated by a local oscillator (LO) because the LO frequency is centered in the wanted channel useful signal and noise occupy both the upper and lower sidebands. Finally, by filtering we would have amplified signal at the wanted frequency. It shows in Figure 1 that the

schematic front-end receiver [20], [23], [55].

In this paper, we present a low-power, high-gain and small-area 24GHz LNA and mixer which are the most important of the front-end receiver for the short-range automotive radar. The proposed circuit is fabricated using 65nm CMOS technology with a supply voltage of 1.5V. The proposed circuit is designed using a low power differential LNA connected to down-conversion mixer including the Gilbert Cell to reduce power consumption and improve the linearity of the front-end received [43], [56].

4.2 Differential Cascode LNA Design Procedure

In this part, the Single-ended LNA architecture has at least one important short coming, and that is its sensitivity to parasitic ground inductance. It is clear from the schematic of Figure 4.1 that the ground return of the single source is supposed to be at the same potential as the bottom of the source degenerating inductor [6]. In order to make a differential LNA circuit, two single-ended circuits built, where each transistor and circuit component has a complementary transistor or component. The positive input voltage is measured at the gate of one of the half-circuit CS amplifiers, while the negative input voltage is measured at the gate of the other half-circuit. The overall output of the LNA is measured between the sources of each half-circuit.

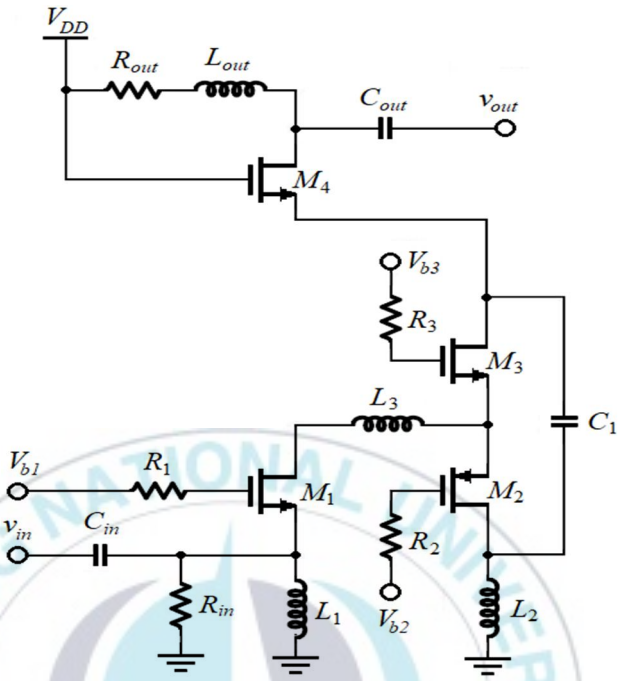


Figure 4.1 Single-ended LNA

Successful integration of the LNA at 24GHz depends on minimization parasitic capacitances and losses to maintain adequate gain, designing with low voltage swing for low breakdown devices, and achieving sufficient linearity required for low spectrally efficient and variable envelope modulation scheme. Providing a resistive input impedance of 50 Ohm is one critical requirement of an LNA. The 50 Ohm termination is required mainly by the previous band select filter L_3, a transistor which is biased and adding parasitic capacitance to the input and has changed the input matching of the

LNA. The third order nonlinearity g_{m3} is performed by gate drain and gate-source capacitances have mixed by basic components, therefore, reduces linearity performance and a little improvement have obtained. For overcome these defects, we proposed a CG NMOS-PMOS inverter for the cascode LNA as alike linearizer. The proposed linearization method accepts NMOS and PMOS transistors into common gate configuration to annul the second-order and third-order nonlinearity at the same time to improve the linearity performance [57]. It is important to keep in mind that for equal total power consumption the noise figure of this amplifier is higher than its single-ended counterpart. Specifically, the power consumed is double that of a single-ended amplifier [58], [59].

4.3 Double-balanced down-conversion Mixer

In this section, the mixer converts the input radio frequency (RF) 24GHz to an intermediate frequency (IF) 2.4GHz. The influence of the mixing stage of the down-conversion mixer as shown in Figure 4 on linearity has been previously investigated in the literature [58]. The output of the down-conversion mixer is taken at the IF- and IF+ terminals. The load resistor is fixed in order to improve the gain of the amplifier. It depends on a great extent on the frequency of operation. At a high frequency where the

parasitic capacitance associated with the transistors are very important. The low voltage ability of the trans-conductor is accomplished through offsetting the gate bias voltage of M_7 & M_8 (M_9 & M_{10}) to ensure simultaneously high input voltage domain for M_7 & M_8 (M_9 & M_{10}) at the supply of 1.5V. The design implements synchronous performance of M_7, M_8, M_9, & M_{10} at the saturation region by a comparatively large domain of the input signal levels. Parallel resistances (R_4=R_5) across a capacitor (C_4=C_5) will force some current and offers a feedforward possibility for the input signal, enhances the high-frequency implementation of the floating voltage source.

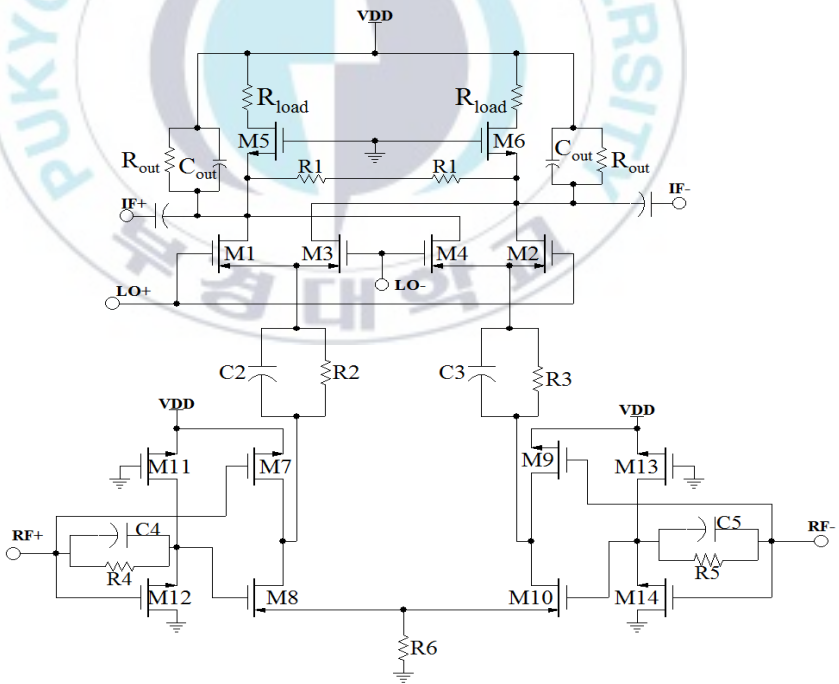


Figure 4.2 24 GHz CMOS down-conversion mixer

Two critical specifications for mixers are low power consumption and low voltage operation. Low voltage mixers are challenging because conventional mixers depend on several transistor scaling [60]. Firstly, circuits configured with sub-threshold region biased MOS transistors operate with lower headroom voltage, leading to lower power supply and thus decreased dc power dissipation [61]. Operating the mixer transistors in subthreshold inversion region provides another advantage. For this conclusion that all switch transistors have constant transconductance (g_m) in the inversion of the subthreshold; the noise efficiency would be greatly enhanced according to strong inversion. RF frontend produces two forms of noise. First of all, flicker noise that is inversely proportional to the size of the transistor and a weakly inverted transistor would be significantly greater than a transistor that is strongly inversed. Secondly, thermal noise is decreased due to the importance of the drain thermal noise factor (γ), which is around 25% lower in weak inversion [62]. In the meantime, the required LO signal power is considered lower in the subthreshold region, and this results in reduced the dc power consumption of LO signal generator.

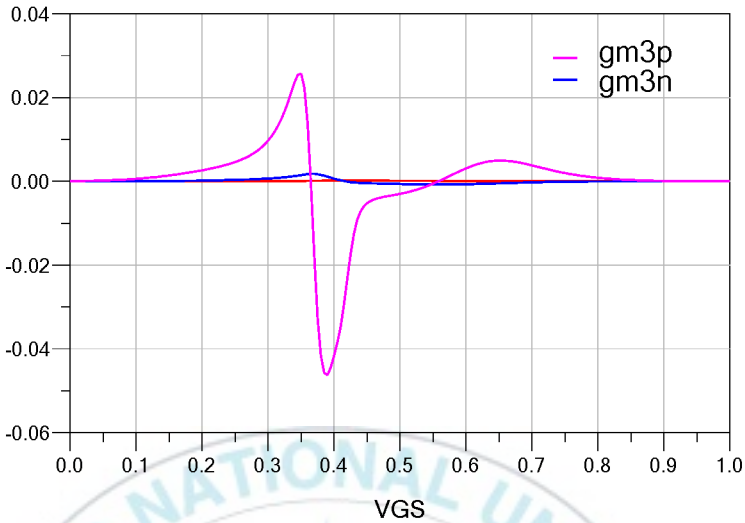


Figure 4.3 Simulated g_{m3n} and g_{m3p}.

4.4 Analysis of the Proposed Front-End Receiver

The regulation activity for automotive radar introduced in the 90s with the allocation of the 76GHz and 77GHz band for LRR system, and then in 2001, Federal Communications Commission (FCC) started the regulation for 24GHz SRR sensor in the US. The short-range radar (SRR) works in pulse mode with a covered distance of about 30 meters and it uses wide bandwidth. Radar for vehicle applications usually uses two frequencies 77GHz and 24GHz, to increase the safety of the future car and avoid an unnecessary collision. Also, 24GHz radar is easier to handle and it is the most used frequency but 77GHz is also considered. The SRR could cover a lot of applications such a parking aid, ACC with stop and go, pre-crash or

collision warning, back-up function. It has also better performance in azimuth angle and in range measurements, thus suitable for automotive applications like parking aid, pre-crash detection, side object detection, and blind spot detection. As describes in Figure 4.4

Figure 4.4 Possible application for automotive radars

4.5 The Proposed Front-End Receiver

The design of merged LNA+mixer architecture, the LNA and mixer combination is on the same chip with a short-range, RF input signal of 24GHz into the LNA in the receiver the signal is amplified at the LNA stage and amplified signal passed into the mixer which is fed by an LO signal of 21.6GHz, and the down-conversion IF signal of 2.4GHz. The first element of the receiver is the antenna which receives the range of frequency coming from the wireless channel. The antenna receivers the signal which may contain added noise along with desired RF signal. After the RF antenna, the

RF bandpass filter allows the required message signal to go through to the front-end of the receiver. We need to consider the effect of the input capacitance of RF transistor of the mixer in the output of the LNA. Additionally, it is possible to add a coupling capacitance to block DC and to be shorted in AC. As shown in Figure 4.7 the whole circuit, the differential LNA is connected to the mixer. This structure provides an excellent voltage gain and noise figure (NF).

At this stage, the channel modulation effect can arise, as shown in Figures 4.5 and 4.6: small variations in length L indeed act as inverse ratios in the current I_{DS} equation below:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right) \tag{4.1}$$

with C_{ox} the surface capacitance of the gate-channel of a MOS transistor, V_{th} its threshold voltage and μ_n the mobility of the carriers.

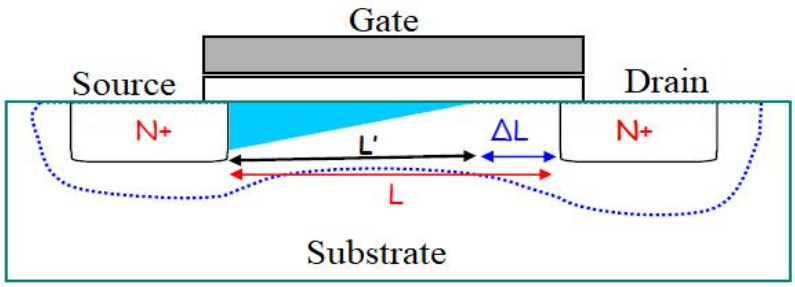


Figure 4.5 Modulation of L when V_{ds} varies

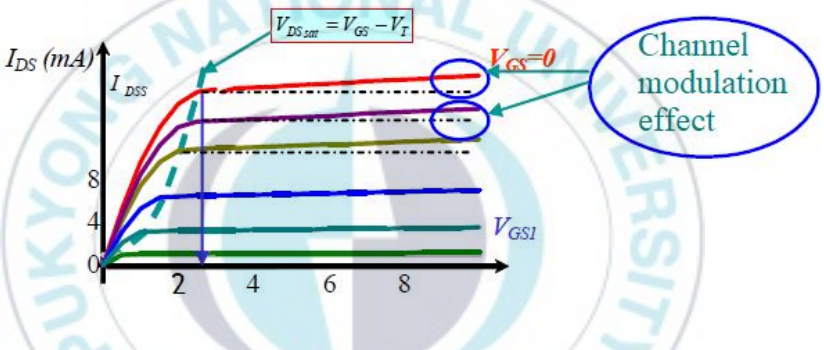


Figure 4.6 Saturation of the MOS as a function of L

At saturation, the more *VDS* increases, the more *L* is reduced on the side of the drain, the potential of which is much more positive compared to the region close to the source, which in fact reflects the nonlinearity of the NMOS.

At saturation I_{DS} checks:

$$\frac{\partial I_{ds}}{\partial V_{ds}} = 0 \tag{4.2}$$

So by deriving equation (4.1) with respect to V_{ds} and canceling the result obtained, we deduce:

$$V_{ds} = V_{gs} - V_{th} \tag{4.3}$$

(4.1) will then be written:

$$I_{DS} = \mu_n C_{ox} \frac{W}{2L} \left(V_{gs} - V_{th}\right)^2 \tag{4.4}$$

$L' = L - \Delta L$ being the effective length of the channel, therefore:

$$I_{DS}{}' = \mu_n C_{ox} \frac{W}{2L'} \left(V_{gs} - V_{th}\right)^2 \tag{4.5}$$

$$I_{DS}{}' = \mu_n C_{ox} \frac{1}{2} \left(\frac{W}{1 - \frac{\Delta L}{L}} \right) \times \frac{1}{L} \left(V_{gs} - V_{th} \right)^2 \quad (4.6)$$

$$I_{DS}{}' = I_{DS} \frac{1}{\left(1 - \frac{\Delta L}{L} \right)} \quad (4.7)$$

Using the empirical relation: $1 - \frac{\Delta L}{L} \cong 1 - \lambda V_{DS}$ (because it is V_{ds} which determines the ΔL displacement of L) and if $\lambda V_{DS} << 1$ (λ being the modulation factor of L) then:

$$I_{DS}{}' = I_{DS} \frac{1}{(1 - \lambda)} \quad (4.8)$$

$$I_{DS}{}' = I_{DS}(1 + \lambda V_{DS}) \quad (4.9)$$

The saturation current finally becomes:

$$I_{DS}{}' = \mu_n C_{ox} \frac{W}{2L} \left(V_{gs} - V_{th} \right)^2 (1 + \lambda V_{DS}) \quad (4.10)$$

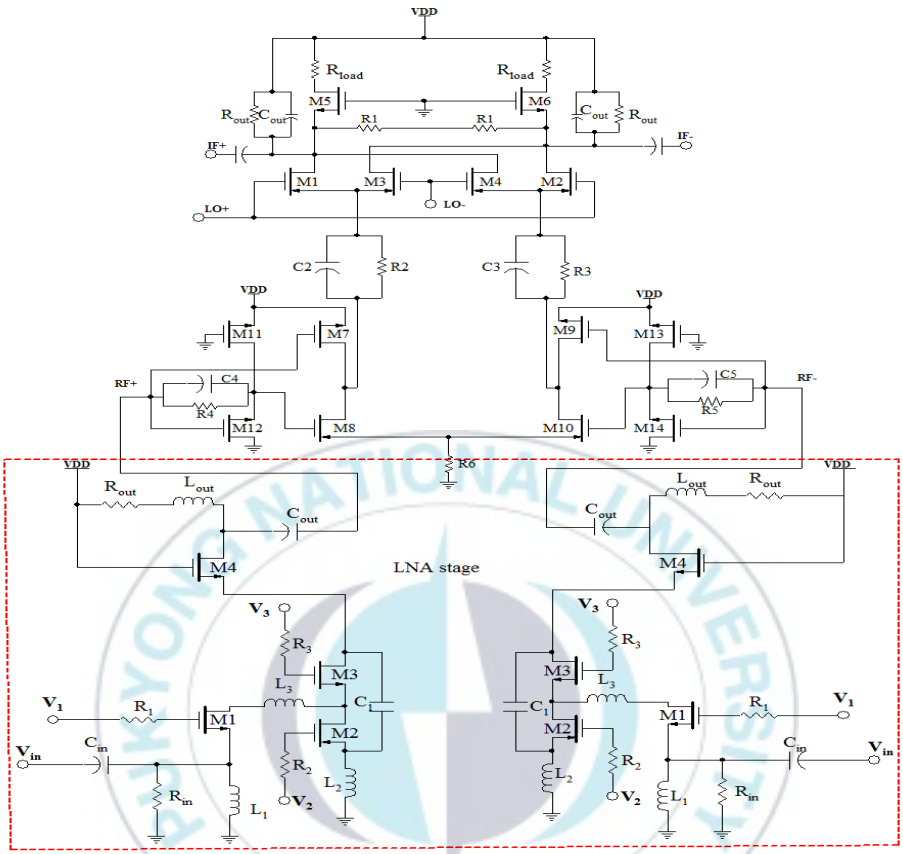


Figure 4.7 Proposed differential LNA connected to down-conversion mixer

However, it should not be too large because larger transistors have a higher gate-source parasitic capacitance which tends to limit the high-frequency operation and increases the noise figure. The half circuit and consisting of M_7, M_8, M_{11}, & M_{12} these various values of the offset voltage of $V=500mV$, for $(W/L)_7$=20μm/0.13μm and $(W/L)_8$=15μm/0.13μm. As described, the RF transconductor is combined to LO (local oscillator) stage

prepared by cross-coupled differential inputs which are ended up in a low pass load to eliminate any unwanted high-frequency composition in the IF (intermediate frequency) signal.

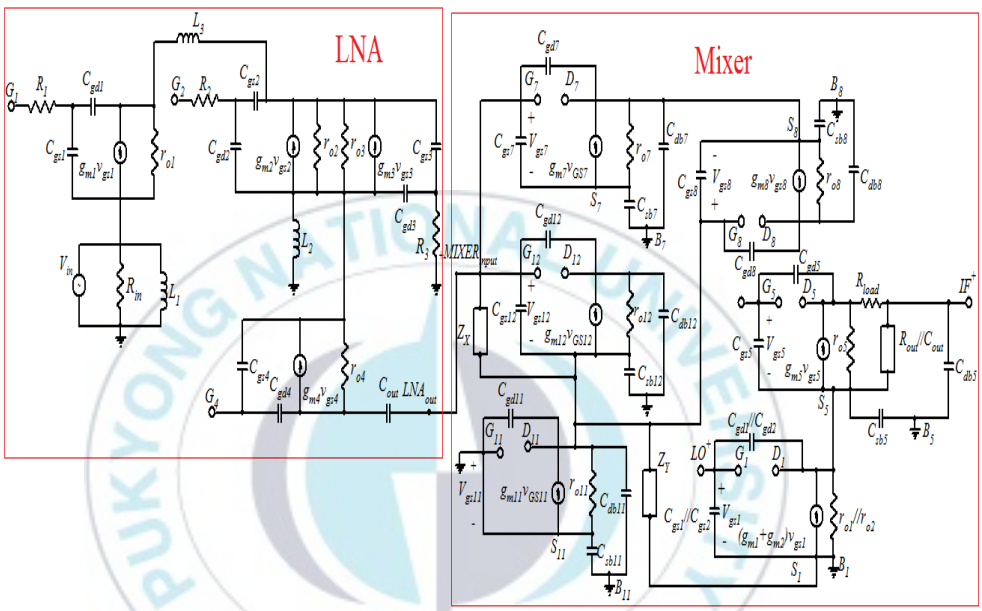


Figure 4.8 Small signal half-circuit model of the proposed LNA-mixer

Figure 4.8 shows the simplified high-frequency small signal model for the positive input side of the LNA- mixer. By applying the KCL at source node s_1 we get

$$I_{in} = \frac{V_{s1}}{R_{in}} + \frac{V_{s1}}{jwL_1} - g_{m1}V_{gs1} - \frac{V_{ds1}}{r_0} - V_{ds1}jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}\right)) \quad (4.11)$$

$$I_{in} = V_{s1}\left(\frac{1}{R_{in}} + \frac{1}{jwL_1}\right) - g_{m1}V_{gs1} - V_{ds1}\left(\frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1}+C_{gs1}}\right)\right) \quad (4.12)$$

$$I_{in} = V_{s1}\left(\frac{1}{R_{in}} + \frac{1}{jwL_1} + g_{m1} + \frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1} + C_{gs1}}\right)\right) - g_{m1}V_{g1} - V_{d1}\left(\frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1} + C_{gs1}}\right)\right) \quad (4.13)$$

Now for AC analysis C_{in} can be shorted, V_{in}=V_{s1} by inserting this value and rearranging, we will get Z_{in} Equation (4.6). A neglecting the term V_{d1} and V_{g1}, using Equation (4.11) and (4.12) we get.

$$I_{in} = V_{in}\left(\frac{1}{R_{in}} + \frac{1}{jwL_1} + g_{m1} + \frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1} + C_{gs1}}\right)\right) \quad (4.14)$$

$$\frac{V_{in}}{I_{in}} = Z_{in} \ (\Omega) \quad (4.15)$$

where the input impedance Z_{in} and output impedance Z_{out} of each stage is optimized at 24GHz and 2.4GHz, respectively. The input impedance of the proposed LNA can be analyzed using the small-signal circuit as given in Equation (4.16).

$$Z_{in} = \frac{1}{\left(\frac{1}{R_{in}} + \frac{1}{jwL_1} + g_{m1} + \frac{1}{r_0} + jw\left(\frac{C_{gd1}C_{gs1}}{C_{gd1} + C_{gs1}}\right)\right)} \quad (\Omega) \quad (4.16)$$

where w is the operation frequency, C_{gd1} and C_{gs1} are the parasitic capacitance of the nMOS.

For Z_{out} is the output impedance of combined the LNA-mixer. By applying the KCL at source node S_5 we get

$$I_{out} = g_{m5}V_{gs5} + \frac{(V_o - V_{s5})}{r_{o5}} + (V_o - V_{s5})jwC_{out} \tag{4.17}$$

$$V_{s5} = I_{out}R_1//r_{o1}//r_{02}$$

$$V_{gs5} = I_{out} - g_{m5}V_{gs5} - \frac{(V_o - V_{s5})}{r_{o5}} + (V_o - V_{s5})jwC_{out} \tag{4.18}$$

$$V_{gs5}(1 + g_{m5}) = I_{out} - \frac{(V_o - V_{s5})}{r_{o5}} + (V_o - V_{s5})jwC_{out} \tag{4.19}$$

$$V_{gs5} = \frac{I_{out}}{(1 + g_{m5})} - \frac{(V_o - V_{s5})}{(1 + g_{m5})r_{o5}} + \frac{(V_o - V_{s5})jwC_{out}}{(1 + g_{m5})} \tag{4.20}$$

$$I_{out} = I_{out}\frac{(R_1//r_{01}//r_{02})}{R_1} + (g_{m1} + g_{m2})$$

$$\left(\frac{I_{out}}{1 + g_{m5}} - \left(\frac{V_o - I_{out}(R_1//r_{01}//r_{02})}{(1 + g_{m5})r_{o5}}\right) - \left(\frac{(V_o - I_{out}(R_1//r_{01}//r_{02})}{(1 + g_{m5})}\right)\right. \tag{4.21}$$

$$I_{out}\left[1 - \frac{(R_1//r_{01}//r_{02})}{R_1} - \frac{(g_{m1} + g_{m2})}{(1 + g_{m5})} - \frac{(g_{m1} + g_{m2})(R_1//r_{01}//r_{02})}{(1 + g_{m5})r_{o5}}\right.$$

$$\left. - \frac{(g_{m1} + g_{m2})(R_1//r_{01}//r_{02})}{(1 + g_{m5})} - \frac{(g_{m1} + g_{m2})(R_1//r_{01}//r_{02})jwC_{out}}{(1 + g_{m5})}\right]$$

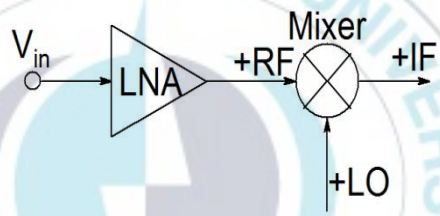
$$= \frac{V_{o(g_{m1}+g_{m2})}}{(1 + g_{m5})r_{o5}} - \frac{V_{o(g_{m1}+g_{m2})}}{(1 + g_{m5})} \tag{4.22}$$

$$V_0\left(\left(\frac{1}{r_{05}}+1\right)\left(\frac{g_{m1}+g_{m2}}{1+g_{m5}}\right)\right)$$

$$= I_{out}\left(\frac{g_{m1}+g_{m2}}{1+g_{m5}}\left[1+\frac{(R_1//r_{01}//r_{02})}{r_{o5}}+\frac{(R_1//r_{01}//r_{02})jwC_{out}}{1}\right]+\frac{(R_1//r_{01}//r_{02})}{R_1}-1\right) \quad (4.23)$$

$$Z_{out}=\frac{\left((R_1//r_{01}//r_{02})\left[\frac{1}{r_{05}}+jwC_{out}+\frac{1+g_{m5}}{(g_{m1}+g_{m2})R_1}\right]+1-\frac{1+g_{m5}}{(g_{m1}+g_{m2})}\right)}{1+\frac{1}{r_{05}}}\ (\Omega) \quad (4.24)$$

The voltage gain of combined LNA-mixer as follows



$$A_{V,Combined}=V_{in}(A_{V,LNA}\cdot A_{V,Mixer}) \quad (4.25)$$

The voltage gain of LNA as given: if we assumed that $r_{01}=r_{02}=r_{03}=r_{04}=r_0$ are same, we will get

$$A_{V,LNA}=g_{m1}g_{m3}g_{m4}\left(\frac{jwL_3r_0}{2jwL_3+r_0}\right)\left(\frac{r_0}{2+r_0g_{m4}}\right)(r_0//R_{out}+jwL_{out}) \quad (4.26)$$

By assuming $r_0=\infty$, therefore we get Equation. (4.27).

$$A_{V,LNA} = g_{m1}g_{m3}g_{m4}(R_{out} + jwL_{out}) \lim_{r_0\to\infty}\left(\frac{jwL_3r_0}{2jwL_3+r_0}\right) \lim_{r_0\to\infty}\left(\frac{r_0}{2+r_0g_{m4}}\right) \quad (4.27)$$

After solving the above Equation (4.27), can be further simplified as follows

$$A_{V,LNA} = g_{m1}g_{m3}g_{m4}(R_{out} + jwL_{out})\frac{jwL_3}{g_{m4}} \quad (4.28)$$

$$A_{V,LNA} = G_T(R_{out} + X_{Lout})(X_{L3}) \quad (4.29)$$

where $X_{Lout} = jwL_{out}$, $X_{L3} = jwL_3$ and $G_T = g_{m1}g_{m3}$

The voltage gain of the mixer as given: because M_5 and M_7 are identical

$$A_{V,Mixer} = \frac{r_{o5}(C_{gd5}-g_{m5})\left(C_{gs5}+C_{bs5}+g_{m5}+\frac{1}{r_{o5}}\right)+(g_{m5}+C_{gs5})(1+\frac{1}{r_{o5}})}{r_{o5}\left(C_{gd5}+C_{db5}+\frac{1}{r_{o5}}\right)\left(C_{gs5}+C_{bs}+g_{m5}+\frac{1}{r_{o5}}\right)+\left(1+\frac{1}{r_{o5}}\right)} \quad (4.30)$$

By rearranging Equation (4.29) and (4.30), we get a combined voltage gain of LNA-mixer Equation (4.31),

$$A_{V,Combined} = (G_T(R_{out} + X_{Lout})(X_{L3}) + jwL_{out}) \ )$$

$$\left(\frac{r_{o5}(C_{gd5} - g_{m5})\left(C_{gs5} + C_{bs5} + g_{m5} + \frac{1}{r_{o5}}\right) + (g_{m5} + C_{gs5})(1 + \frac{1}{r_{o5}})}{r_{o5}\left(C_{gd5} + C_{db5} + \frac{1}{r_{o5}}\right)\left(C_{gs5} + C_{bs} + g_{m5} + \frac{1}{r_{o5}}\right) + \left(1 + \frac{1}{r_{o5}}\right)}\right) \quad (4.31)$$

4.6 Results and Discussions

The main objective of this work was to design and develop the front-end receiver of an RF in 65nm technology. The incoming RF signal was at 24GHz which was then down-converted to a low IF signal. The whole schematic of the proposed LNA-mixer is depicted in Figure 4.7 using Cadence Spectre-RF and Calibre platform software is implemented in a 65nm CMOS process for the automotive collision avoidance radar of 24GHz. Simulations are carried out with the supply voltage of 1.5V and at a temperature of 27° The RF input of the LNA is matched to 50 Ohm termination through cascode inductive source degeneration and respective simulated input return loss is illustrated in Figure 4.11.

4.6.1 Transient signal

Figure 4.9 gives the frequency spectrum of V_{RF} and V_{IF}. The presence of a harmonic balance at RF and LO frequencies are respectively, 24GHz and 21.6GHz which provides an IF frequency of 2.4GHz for front-end receiver. The differential input and output voltage amplitudes in a transient analysis are depicted in Figure 4.9. Based on the data from the peak-markers, we can estimate the voltage gain of this mixer as: $G_V = 20\log(\frac{V_{(RF-LO)}}{V_{(RF)}})$

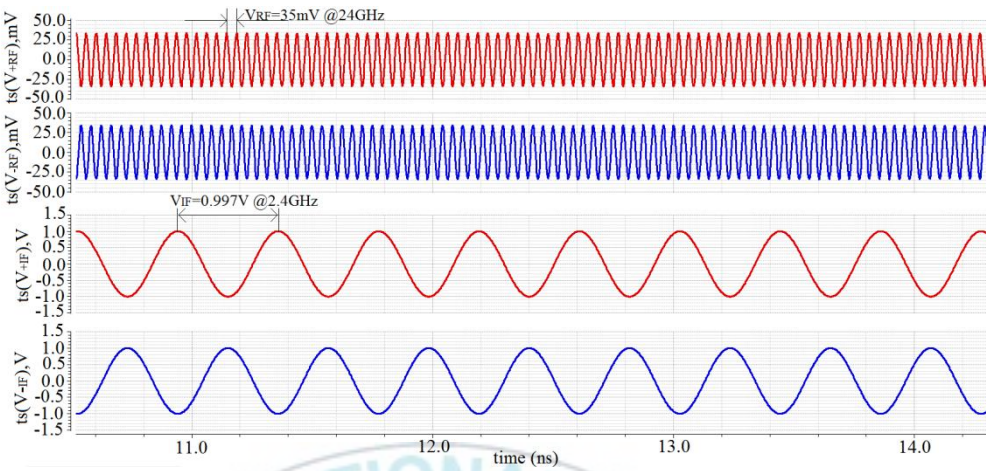


Figure 4.9 Input and Output signal

4.6.2 Power consumption

For getting the power consumption DC simulation is performed, the integrated LNA and mixer dissipate the 4.028mW, with the supply voltage of 1.5V.

4.6.3 Harmonic response

The following Figure 4.10 shows that the output a frequency of RF-LO value equal to 2.4GHz. The proposed circuit showed the highest conversion gain of 28.1dB as compared to recently reported research results. This reveals the importance of taking into consideration all the internal CMOS parameters which are responsible for measurable results.

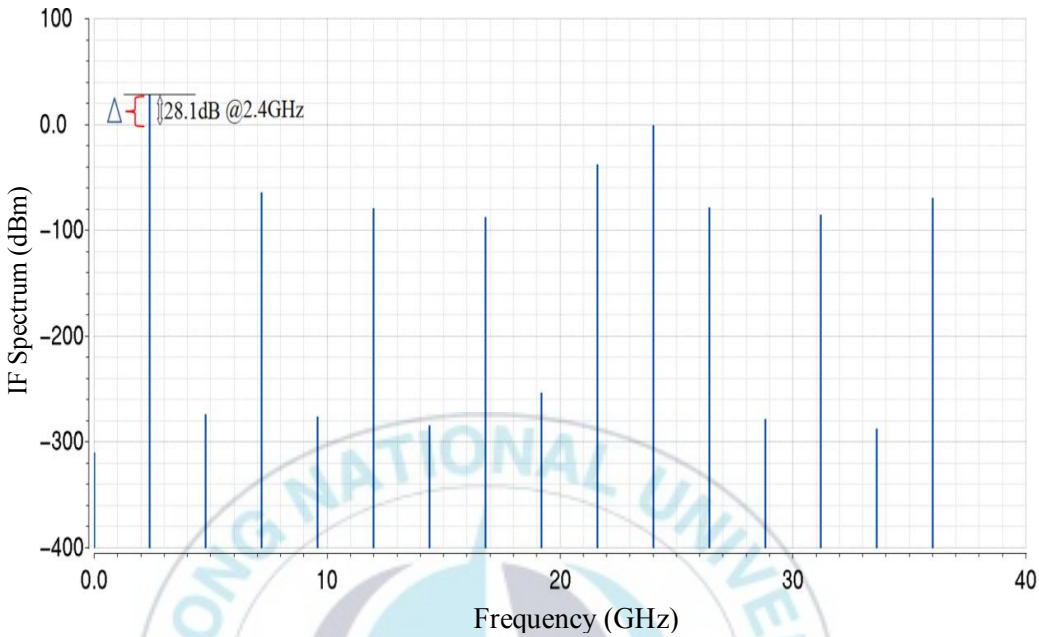


Figure 4.10 Conversion gain of proposed LNA-mixer

4.6.4 S-Parameter response

Figure 4.11 shows us the combined condition of the input return loss of more than -28.5dB rejection at 24GHz operating frequency confirms the matching obtained. Also, the output return loss S_{22} is -28.0dB around 2.4GHz. The RF input and RF-LO output are good matched at their respective frequencies. The voltage gain of the LNA is 24.3dB at 24GHz.

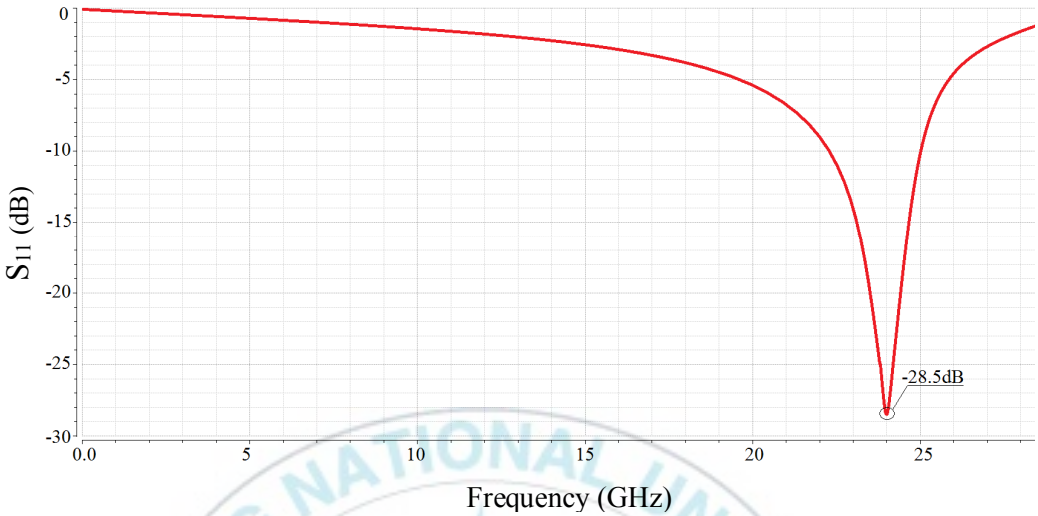


Figure 4.11 Simulation result of input S_{11} loss

4.6.5 Noise Figure

The simulated noise figure of the combined LNA-mixer is about 3.66dB at 24GHz, the noise figure and gain of the first stage are very important contributions to the total noise figure. A large gain and a small noise figure for the LNA in a system should be significant considerations for good signal processing.

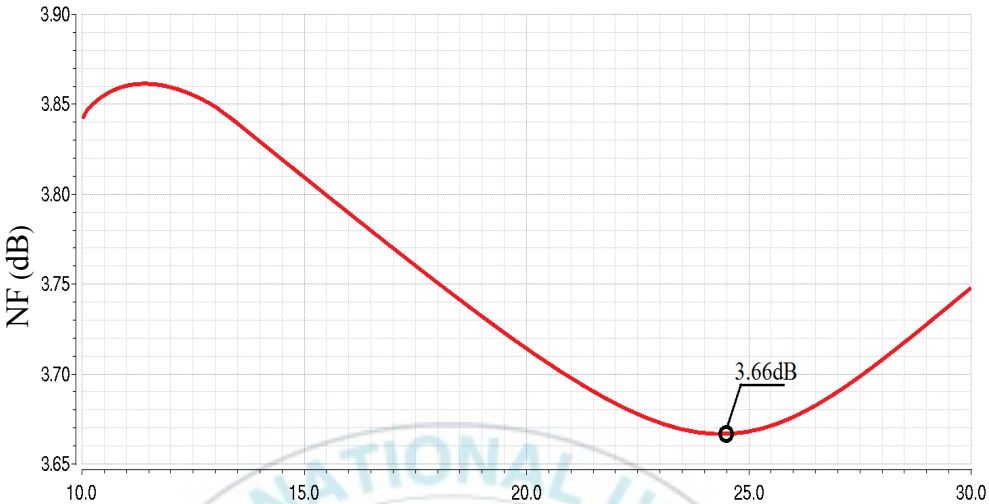


Figure 4.12 Simulation result of noise figure

The die layout is depicted in Figure 4.13. The proposed 24GHz LNA-mixer is implemented in 65 nm CMOS process. The size of the die of designed LNA-mixer is $0.800\times120mm^2$ including pads and $0.322\times0.899mm^2$ without pads. The RC capacitors 2.5pF combinations employed System-On-Chip at the supply voltage. All resistors and capacitors are implemented using P+Poly Salicide-Resistor (*ppcres*) and 2-Node-Metal-Insulator-Metal-Capacitor.

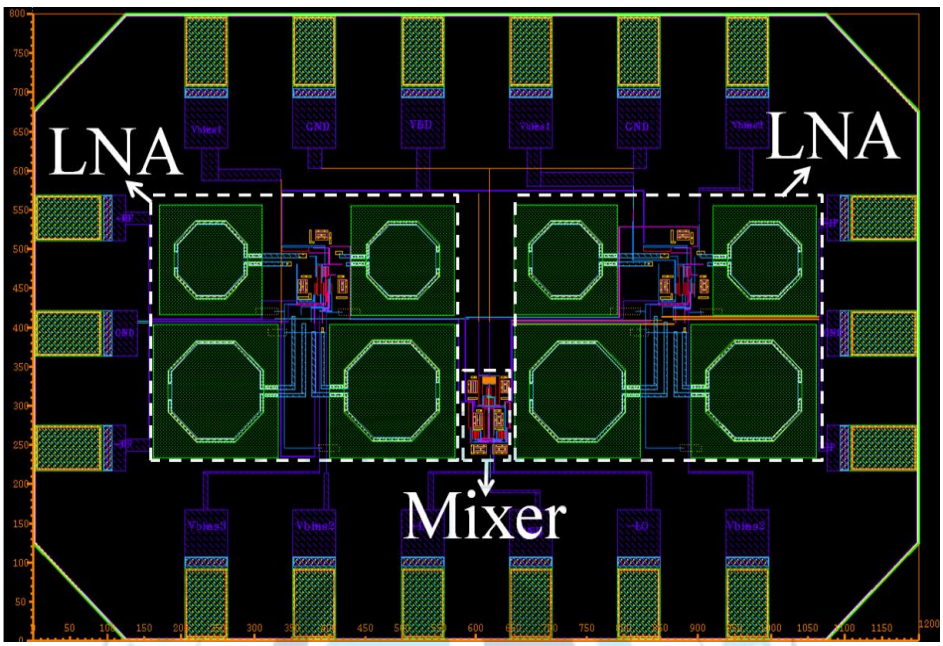


Figure 4.13 Layout of front-end receiver

Table 4.1: Measured results for the receiver front-end

Supply Voltage		1.5V
Technology		65nm CMOS
RF frequency		24GHz
IF frequency		2.4GHz
LNA	Voltage gain	24.3dB
	Noise figure	2.93dB
	S11/S22	-32.8/-32.7dB
	IIP3	3.2dBm
	Power consumption	4.59mW
	Chip area	0.32x0.40mm^2
Mixer	Conversion gain	14.8dB
	Noise figure	2.87dB
	S11/S22	-29.74/-29.92dB
	IIP3	3.2dBm
	Power consumption	1.54mw
	Chip area	0.10x0.10mm^2
Receiver	Conversion gain	28.1dB
	Noise figure	3.66dB
	S11/S22	-28.5/-28.0dB
	IIP3	4.50dBm
	Power consumption	6.043mW
	Chip area	0.80x1.2mm^2

Table 4.2: Shows the comparison of this work and some of the 24GHz front-end receiver reported in the recent literature

Comparison Table				
Parameters	**This Work**	[65]	[66]	[67]
Frequency (GHz)	**24**	24	24	24
Voltage gain (dB)	**28.1**	28.4	27.5	20.7
Input Return loss S_{11} (dB)	**-28.5**	-14.3	-21	-17
Power consumption (mW)	**6.04**	54	64.5	38.5
Noise Figure (dB)	**3.66**	6.0	7.7	7.8
CMOS Process (nm)	**65**	180	1800	130
IIP3 (dBm)	**4.50**	-13.0	-	-
Supply voltage (V)	**1.5**	1.8	1.5	-
Chip area mm^2	**0.80×1.2**	1.1x1.2	0.4x0.5	5x5

4.7 Summary

In this paper, we have proposed a differential LNA is merged with double-balanced mixer for the automotive collision avoidance radar of 24GHz. It was successfully designed and verified using Cadence 65nm CMOS process. Thanks to the cascade inductive source degeneration technique and the bias offset method with the elimination of tail current shaping transistors. According to the experimental results, the LNA offers a gain of 24.3dB and NF is 2.93dB with power consumption of 4.59 mW from the supply voltage of 1.5V, the simulating double-balanced mixer conversion gain of 14.8dB and noise figure of 2.87dB.

The proposed RF front-end blocks were a low noise amplifier (LNA), down-conversion mixer, combination operates at 24GHz. The LNA-mixer were connected together to form a receiver. The results obtained from the simulation by HSpice RF are depicted in Figure 4.9 - 4.12. To observe the change in the behavior of the circuit because of the variation of fabrication parameters, process corner (slow, fast and typical) simulation was carried out in Cadence Spectre. It is shown in Figure 4.11 the input return loss (S_{11}) of -28.5dB at 24GHz, the noise figure of 3.66dB and overall conversion gain of 28.1dB is obtained at 24GHz. The proposed front-end receiver,

power consumption and the third order intercept point (IIP3) are 6.043mW and 4.50dBm respectively. The size of the die of designed merged LNA-mixer is 0.80x1.2mm^2 including pads. Table 4 shows the comparison of this work and some of the 24GHz front-end receiver reported in the recent literature. Hence, the front-end receiver is suitable for low power and high-frequency application such as a short-range radar system.

Chapter 5

5. Conclusions and Future work

5.1 Conclusion

In many transport and luxury passenger cars, radar prevention systems are now mounted to increase protection. These radar-based instruments are implemented in a receiver interface to accomplish the predefined objectives. Several blocks of transceivers have recently been mounted on the single chip to increase the degree of integrity. This dissertation focused on issues surrounding the design of a development of low-voltage high linearity CMOS RF frontend technology for automotive collision avoidance radar. This chapter summarizes the work presented in this dissertation and concludes with a discussion of future research topics.

Summary and Contributions:

In chapter 2 a low-power low-noise 24-GHz CMOS LNA for automotive collision avoidance radar is designed. The cascode inductive source degeneration technique is used to design LNA. To improve noise figure and linearity, the CG (common gate) NMOS-PMOS inverter scheme for the cascode LNA as a linearizer. The proposed linearization method

accepts NMOS and PMOS transistors into common gate configuration with the second-order and third-order nonlinearity to improve the linearity performance. The proposed circuit is fabricated using 65nm RF CMOS technology, and it is powered by1.5V supply. To increase voltage gain and decrease power consumption. The proposed LNA showed the lowest power consumption of 4.59mW and the lowest noise figure of 2.98dB with high voltage gain of 24.3dB as compared to recently published results.

In chapter 3, a low power 24GHz (RF) down-conversion mixer including the Gilbert Cell for short-range automotive radar system is designed. The mixer is implemented using 65nm RF CMOS technology. The mixer is designed using a bias offset method to have high conversion gain, improved the linearity and reduced power consumption. The conversion gain and noise figure mixer is 14.8dB and 2.87dB respectively. The mixer consumes power of 1.57mW at 1.5V supply voltage.

In chapter 4, RF front-end, the differential LNA merged along with a double balanced mixer is designed, for the 24GHz automotive collision avoidance radar. The RF front-end is designed with the help of the cascode inductive source degeneration technique and the bias offset method and the results are simulated and verified by using Cadence 65nm CMOS process.

The results obtained from the LNA, mixer and Front-End Receiver studied in this work present very acceptable performances in a wide frequency band, this circuit thus designed indeed displays good values of gain, compression points and interception of order IIP3 very large in the whole operating frequency range, which justifies the excellent linearity of this topology, also we obtained a very low noise figure, i.e. 3.66dB and good isolation, less than -10dB, all this with an acceptable power dissipation not exceeding 6.04mW. Table 4 above shows a possible comparison with the results obtained in recent work.

Finally, we have detailed the performance of each circuit by specifying the design details and the reasons that motivated certain topology choices, in particular for the IF amplifier with a theoretical analysis of the feedback. The simulated performance of the frequency converter is finally presented.

5.2 Future work

The automotive industry is working to reach the target of zero deaths associated with vehicle, as well as to satisfy customer demand and public law, pushing innovative vehicle safety technologies. The government is expected to provide specialized driver assistance (ADAS), radar and camera systems in future. This radar solution provides long- and medium-range

features which enable car systems to track the vehicle's environment to prevent crashes. Freescale's multi-channel radar system is made up of transmitter and receivers that permit high-level integration and complex signal generation and processing.

The key aim of this dissertation is the design of high-performance, front-end building blocks, together with low-noise amplifiers (LNA) and down-conversion mixers, and does not cover the implementation of a complete receiver. Challenges remain in designing a completely reconfigurable, low-cost, multi-band, multi-standard receiver chip, at both the system and circuit levels. Hence, there are ways to improve the performances. Some of the circuits can be changed in design and optimized to have better results. Moreover, a receiver needs a highly reconfigurable frequency synthesizer that can be adjusted for various output frequencies, bandwidths, and phase noise levels. Another interesting topic for research would be the high-level implementation of a complete front-end to improve overall noise, linearity, and selectivity. The other interesting topic could be designing a low-cost, multi-band, mixed-signal front-end with digital interface and calibration would make significant contributions to this field of study. However, the acquired knowledge from this thesis work can help to design the whole RF receiver system in the 24GHz band.

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[Appendix]

Publication Paper List

(1) Journal

Paper Title	Date	Journal Title
Development of Low-Power Low-Noise CMOS LNA for 27-GHz Automotive Radar	April 2020	Journal of Semiconductor Technology and Science (SCIE)
Low-Power low-phase noise VCO for 24 GHz application	February 2020	Microelectronics Journal (SCIE)

(2) Conference

Paper Title	Date	Conference Title
Development of Low-Noise CMOS LNA for 24-GHz Automotive Radar	December 2020	Proceedings of 2020 Symposium on the Institute of Electronics and Information Engineers
A 24 GHz High Gain, High Efficient Stagger-Tuned CMOS Power Amplifier	December 2020	Proceedings of 2020 Symposium on the Institute of Electronics and Information Engineers
Design of Variable Gain Amplifier with Active Inductor	December 2020	Proceedings of 2020 Symposium on the Institute of Electronics and Information Engineers
Design of a High-SNDR 12-bit 1MSps Fully-differential SAR ADC	December 2020	Proceedings of 2020 Symposium on the Institute of Electronics and Information Engineers
A 24-GHz Low Voltage High Gain Up-Conversion CMOS Mixer for 5G Applications	December 2020	Proceedings of 2020 Symposium on the Institute of Electronics and Information Engineers

Design of A Low Voltage, Low Phase Noise, and Wide Tuning Range LC Tuned VCO with A DAI	December 2020	Proceedings of 2020 Symposium on the Institute of Electronics and Information Engineers
Hardware Realization of Pattern Recognition using Spiking Neural Network	December 2020	Proceedings of 2020 Symposium on the Institute of Electronics and Information Engineers
Low Noise Amplifier in Neural Signal Analysis : Advances and Challenges	June 2020	2020 ICT 대학생 논문 경진 대회
A Small Ripple Voltage Doubler Charge Pump Circuit with Improved Pumping Efficiency	June 2020	2020 ICT 대학생 논문 경진 대회
Two-Stage High-Gain 24GHz CMOS Power Amplifiers with pMOS and nMOS	June 2020	Proceedings of the 2020 KSPSE Spring Conference
A Low-Noise High-Linear CMOS Up-Conversion Mixer for 24GHz Applications	June 2020	Proceedings of the 2020 KSPSE Spring Conference
24-GHz Low-Power VCO for Automotive Radar Application	December 2019	Proceedings of 2019 Symposium on the Institute of Electronics and Information Engineers
Design of a 24-GHz high performance class AB CMOS power amplifier for wireless applications	December 2019	Proceedings of 2019 Symposium on the Institute of Electronics and Information Engineers
Design of Low-Power 12-bit 1MSps SAR Analog-to-Digital Converter	December 2019	Proceedings of 2019 Symposium on the Institute of Electronics and Information Engineers
Development of Pattern Generation Module for High Resolution 3D Scanner	November 2019	Proceedings of the 2019 KSPSE Autumn Conference

Portable Small High-Precision Hardness Tester	November 2019	Proceedings of the 2019 KSPSE Autumn Conference
GHz-Band Low Noise Amplifier with Improved Linearity	October 2019	Proceedings of Conference on Information and Communication Engineering
Design of Programmable Finite Impulse Response Filter	October 2019	Proceedings of Conference on Information and Communication Engineering
Ultra-Low-Noise Low-Power VCO for 24GHz Application	June 2019	Proceedings of 2019 Symposium on the Institute of Electronics and Information Engineers
Design of Programmable Gain Amplifier	June 2019	Proceedings of 2019 Symposium on the Institute of Electronics and Information Engineers
Mixer Design of High Conversion Gain and High Linearity for 24GHz Application	June 2019	Proceedings of 2019 Symposium on the Institute of Electronics and Information Engineers
A Low-Noise Low-Power Down-Conversion Mixer in 130nm RF CMOS Technology for 24GHz Application	May 2019	Proceedings of the 2019 KSPSE Spring Conference
Manchester-Coded Code Shift Keying Modulation Scheme in Visible Light Communication	May 2019	Proceedings of the 2019 KSPSE Spring Conference
Realization of Portable High-Precision Hardness Tester	May 2019	Proceedings of the 2019 KSPSE Spring Conference
Design of 77-GHz CMOS Voltage-Controlled Oscillator with Low-Phase Noise	May 2019	Proceedings of Conference on Information and Communication Engineering
Design of Programmable Finite Impulse Response Filter	May 2019	Proceedings of Conference on Information and Communication Engineering
A Low Noise Amplifier	December	Proceedings of 2018

Design and Optimization	2018	Symposium on the Institute of Electronics and Information Engineers
Design of Power Amplifier for Automotive Long Range Radar	December 2018	Proceedings of 2018 Symposium on the Institute of Electronics and Information Engineers
Design of 24GHz Differential Low-Noise Amplifier Using TSMC 130nm RF CMOS Technology	November 2018	Proceedings of the 2018 KSPSE Autumn Conference
Design of 77GHz Power Amplifier	November 2018	Proceedings of the 2018 KSPSE Autumn Conference
A Low Power 24GHz LNA using 0.13μm CMOS Process	June 2018	Proceedings of 2018 Symposium on the Institute of Electronics and Information Engineers
Design of Low Power 24GHz CMOS VCO	June 2018	Proceedings of 2018 Symposium on the Institute of Electronics and Information Engineers
Realization of Programmable Digital Filter for Noise Cancellation	June 2018	Proceedings of Conference on Information and Communication Engineering
Low-Phase Noise 24-GHz CMOS Voltage-Controlled Oscillator	June 2018	Proceedings of Conference on Information and Communication Engineering
Design of LNA for 24 GHz CMOS Application	December 2017	Proceedings of 2017 Symposium on the Institute of Electronics and Information Engineers
24GHz TSPC Frequency Divider for CMOS Application	December 2017	Proceedings of 2017 Symposium on the Institute of Electronics and Information Engineers

Low-Noise-Amplifier LNA 24 GHz CMOS Application	June 2017	Proceedings of 2017 Symposium on the Institute of Electronics and Information Engineers